Cynergy4MIE

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Bridging Ecosystems for European Technological Advancement

Deliverable	**Components and Circuits for safe and efficient e-drives, high performance battery with advanced BMS and WBG power inverter systems**		
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1 Executive publishable summary

In this deliverable, partners relate about the developments carried out and the results achieved in the development of five different demonstrators in the scope of the use cases of traction and auxiliary e-drive systems, advanced battery management for a high-voltage mobile battery application, the application of WBG SiC and GaN components in power electronics, and advanced software development technologies.

As such, this deliverable describes the activities of the SC3 - partners in the work package WP3 of the Cynergy4MIE project, and the partial results achieved so far.

2 Non publishable information

In Demo 3.1, ZF decided to work with a different motor than originally planned in the project proposal. The initial plan was to use a high-voltage powertrain with a PMSM. However, they proposed working with a low-voltage AC induction motor. The aim is to use magnetic flux sensors and integrate them into the motor to estimate the rotor position based on the measurements and thus replace the position sensor in the control loop.

This change was further accompanied by other consequential changes, because the utilisation of a high-voltage inverter would have led to low efficiency and possible problems with demonstrating the benefits of the proposed solution. Therefore, I&M proposed to use their existing low-voltage (48 V) inverter and supported this demo with the target of adapting the software from Permanent Magnet Synchronous Motor (PMSM) motor control to AC Induction Motor (ACIM) motor control.

This approach was communicated with an approved Amendment. I&M increased their involvement in the project (in Demo 3.1) by taking over part of the budget from BELGAN.

Another change in Demo 3.1 was caused by confidentiality issues between the involved partners. ZF could not provide all information about the new motor to AVL due to confidentiality, which made it impossible to carry out Finite Elements Method (FEM) simulations as originally planned. The university partner BUT, who had initially planned to cooperate with AVL on simulations, took over these activities, and AVL redirected their efforts to Demo 3.3 instead.

There were also other changes related to BELGAN, who withdrew from the project in its initial phase. This influenced Demo 3.4, but the issues are resolved as I&M took over part of BELGAN effort and found alternative electronic power components on the open market.

Demo 3.5 referenced in this deliverable was not originally mentioned in the GA and will also require a new amendment. Partners TUE and VER were originally involved in Demo 3.2, dealing with batteries and BMS. Showcasing their tool in this demonstrator would not reveal its full potential for the development of complex software.

The new plan is to demonstrate it using an autonomous parcel delivery vehicle, in the newly defined Demo 3.5.

3 Introduction & Scope

3.1 Purpose and target group

The aim of this document is to describe the choices made during the initial phase of development of the demonstrators included in SC3.

The activities related to component development of WP3 are based on the requirements and specifications defined in WP1 and on the system-level design carried out in WP2. Then in WP4 the software will be developed, followed by integration in WP5, and finally in WP6 during the testing phase, where the fulfilment of individual requirements, specifications, and key performance indicators will be evaluated.

Other supply chains and their corresponding tasks use the same taxonomy, which facilitates orientation in the requirements and specifications defined throughout the Cynergy4MIE project contributions of partners.

There are eight partners who directly contributed content to this document, and two partners in the role of associated partners who contributed through discussions and their expertise. They also plan to contribute at a later stage of the project with demonstrations. The individual contributions of the partners are briefly indicated in Table 1.

Chapters	Partner	Contribution
1, 2, 3, 4, 7, 8, 10, 11, 12	I&M	I&M was leading the preparation of this deliverable, contributed with the introductory parts. Major part of the developments in Demo 3.3 and Demo 3.4 is under direct responsibility of I&M, and they also contributed to Demo 3.1 where they will make their 48V inverter available and will later provide the basic control software for the AC induction motor.
5, 10	EDI	EDI contributed with details on components developed for Demo 3.1
6, 10	FAU	FAU was working on the miniaturization and improved sensitivity of the developed quantum sensor, as well as applying the sensor in battery characterization experiments.
5, 10	IFAT	IFAT contributed with details on components developed for Demo 3.1
5, 10	TUG	Graz University of Technology (TUG) designed and built a static and dynamic test bench to develop a novel metamaterial torque sensor and conducted first measurements with each set-up.
6, 10	SAL	SAL designed an experimental battery test setup, investigated the capability of quantum sensors for battery characterization, and developed AI-driven models for SoH estimation.
7, 10	ST-I	ST-I delivered 3D files of their “Gemini modules” evaluation kit.
9, 10	TU/e	The TU/e started with extensive research regard high-band width current sensing and the limitations and possibilities. Additionally, phase-delay compensation is targeted to even further decrease phase delay in the sensor.

TABLE 1: CONTRIBUTIONS OF PARTNERS

3.2 Relation to other activities in the project

This section explains relations and links to other activities in the project. The following inputs and outputs are expected:

Inputs: this document relies on the inputs coming from Deliverable D1.3-T1.3 (describing the requirements, specifications and defined KPIs for the Demos) and all the other working documents coming from WP2 shared within the Cynergy4MIE project (dealing with system architecture design and simulation models). Due to V-cycle model of the project execution, there are also some feedbacks and interactions with WP4 (Task 4.3) where embedded hardware and software is being designed.

Outputs: this document describes the status of development of new electronic components and circuits for powertrains which will be used to build Demos 3.x. Those Demos will be completed in the final year of the project, and a dedicated final deliverable for WP3 (Task 3.2) will be prepared accordingly (D3.4). The work had also already been initiated in WP4, in Task 4.3, developing algorithms and embedded hardware and software for the powertrain based on defined requirements. Finally, realised components will be integrated in WP5 (Task 5.3) and tested in WP6 (Task 6.3) at the end of the project.

Supply chain 3 thus spans through the whole chain of the work packages with planned developments, namely in WP1 to WP6. It also contributes to project management actions in WP7 and WP8. Due to the issues with restructuring SC3, there was not much effort put into seeking synergies with the other supply chains. A potential candidate could be the SC6 due to the utilisation of GaN devices in heat pumps, similarly as in Demo 3.4 for the construction of the inverter.

4 Supply Chain overview

This section describes the motivation for the developments in Supply Chain 3 and briefly describes the planned demonstrators and use cases. It also outlines individual demonstrators from the perspective of the state of the art and potential improvements.

This entire chapter is very similar to that presented in D1.3 as it is intended to be a general overview of Supply Chain scope and to introduce the technical details presented in Chapter 5 to 8, dedicated to the Demonstrators 3.1 to 3.4 (included in WP3 scope).

4.1 Motivation for SC3 and expected outcomes

The global transportation sector is undergoing a profound transformation as the majority of vehicles transition to electrification. This shift requires substantial technological advancements across multiple domains to ensure energy efficiency, system robustness, functional safety, and long-term reliability under diverse operating conditions. To achieve these goals, breakthrough innovations are needed in four key areas: powertrain systems, electric drives, battery architectures, and vehicle electronics. These technologies must be seamlessly integrated and supported by next-generation measurement methods that deliver real-time, precise, and context-aware data for control and diagnostics. Gaining deep insights into component-level performance in real-world environments will be essential for optimising operation and extending service life.

The main technological outcomes envisioned in SC3 include:

- **Demo3.1 - Minimally Invasive Sensors for Efficient, Fail-Safe EV Powertrains** - Next-generation electric drives utilising novel, minimally invasive sensors that enable ultra-high efficiency, high torque precision, improved reliability, and enhanced safety in dynamic operating conditions.
    - **UC3.1.1 – Torque Sensor -** A revolutionary torque sensing concept that exceeds current state of the art, based on tuneable metamaterials that offer both exceptional resolution and high immunity to external electromagnetic fields (EMC resilience).
    - **UC3.1.2 - Motor control without position and speed sensor -** In this demonstrator, the use of additional magnetic flux sensors located in the motor, in combination with other quantities available in the inverter is planned to create a virtual rotor position sensor.
- **Demo 3.2 - Modular, High-Performance, Smart Battery for Mobile Machines -** A modular, AI-enhanced battery system incorporating quantum sensors and connected to a digital twin, enabling both local optimisation and fleet-wide control for improved energy usage, lifecycle management, and fault prediction.
- **Demo 3.3 - SiC Power Inverter for EVs @ 150 kW / 800 V -** The broad adoption of wide-bandgap materials such as SiC and GaN in a wide range of automotive electronics, supporting both high-voltage traction systems and low-power auxiliary circuits, results in greater energy efficiency and component miniaturisation. New packaging technologies for the power modules are exploited in the SiC power inverter to improve both power density and efficiency.
- **Demo 3.4 - Sensor-Enabled GaN Power Inverter for LEVs / Bikes @ 40 kW / 400 V** - In addition to what has already been stated for Demo 3.3, inverters based on wide band gap materials pose new challenges in terms of EMC and motor windings insulation reliability due to their intrinsic

very high switching speed. To mitigate these issues, filtering on both DC and AC side will be addressed in the GaN power inverter.

- **Demo 3.5 - Advancing Software Development Technologies: Autonomous Parcel Delivery Vehicle -** This demonstrator addresses the complexity of software development, which poses a challenge to achieving software efficiency. The novel combination of low-code approaches for embedded software development with formal methods for verifying the correctness of the generated code simplifies the development process and reduces costs.
- **High bandwidth current measurement for advanced control strategies in power converters –** This demonstrator targets the realization of a current measurement with a high bandwidth to enable advanced control strategies that rely on accurate current measurements and/or zero-crossing detection.

The following subsections describe the state of the art of the individual demonstrators and use cases.

4.2 Demo 3.1

UC3.1.1 Torque Sensor - Advancing Torque Sensor Technology for Automotive Applications

In the development of next-generation automotive torque sensors, engineers must balance a complex set of requirements—including accuracy, robustness, miniaturisation, and lightweight design. These criteria are critical for ensuring high-performance operation in demanding vehicle environments, such as in electric powertrains, steering systems, and drivetrains. Despite advancements, current state of the art torque sensing technologies falls short of meeting all these requirements simultaneously.

Limitations of Existing Torque Sensing Technologies

- The predominant torque sensing solutions in use today each face significant limitations that restrict their effectiveness and applicability in modern automotive systems:
- Magneto-elastic torque sensors: These sensors detect torque via changes in magnetic permeability under mechanical stress. However, they are highly susceptible to external magnetic interference, which can distort readings, and their integration into compact designs is challenging, hindering use in space-constrained applications.
- Strain-gauge-based torque sensors: While they can function in a contactless manner, their operation generally involves complex signal conditioning and mechanical setups, leading to bulky and expensive systems. Their complexity increases maintenance and limits scalability.
- SAW (Surface Acoustic Wave) torque sensors: These sensors utilise piezoelectric materials to detect surface wave distortions caused by strain. A major drawback lies in the limited temperature tolerance of piezo ceramics, which are prone to fracture or functional degradation when subjected to strain beyond a critical threshold. This severely restricts their deployment in harsh automotive thermal environments.
- Shift angle measurement techniques: These approaches derive torque indirectly from angular displacement but are vulnerable to external magnetic fields, which compromise measurement accuracy and reliability, especially in electromagnetically noisy environments.

To overcome these shortcomings, the Cynergy4MIE project is pioneering a novel approach by exploring millimetre-wave (mm-wave) based torque sensors. This beyond-state of the art concept

leverages the unique properties of tuneable metamaterials in the mm-wave frequency range to deliver a compact, interference-resilient, and high-precision sensing platform.

The core principle involves the mechanical coupling of torque to a mm-wave metamaterial structure, whose resonant frequency shifts in response to applied strain. This shift alters the phase and amplitude of the reflected mm-wave signals, which are captured using a continuous wave sensor chip. By employing in-phase and quadrature (I/Q) demodulation techniques, the system accurately quantifies amplitude modulation, from which the torque can be reliably calculated.

Key Advantages of the mm-wave Metamaterial Approach

- Immunity to magnetic interference, thanks to the non-magnetic nature of mm-wave signal propagation.
- Scalability and miniaturisation, enabled by the compact size of mm-wave components and metamaterial structures.
- Temperature resilience, as the sensing principle does not rely on fragile piezo materials.
- Simplified system architecture, with fewer mechanical and electronic components compared to strain gauges or SAW systems.

In summary, Cynergy4MIE's development of mm-wave torque sensors represents a transformative step in automotive sensing, with the potential to deliver robust, compact, and high-fidelity torque measurement in a broad range of operating conditions previously inaccessible to conventional sensor technologies.

4.3 Demo 3.2

Battery Management System (BMS) applications for electric vehicles rely on precise State of Health (SOH) estimation to reduce the risk of failures that could lead to safety hazards and to optimise battery performance by enabling adaptive charging and discharging strategies. Electric powertrains, built into electric vehicles, consist of a battery pack made up of multiple battery cells, each exhibiting different behaviours or characteristics. Our previous work includes developing Edge artificial intelligence solutions for battery management [10] and an energy management algorithm for battery sharing [11].

The battery SOH can be calculated by the Coulomb counting method but requires full cycle data and suffers from cumulative error over time. Impedance spectroscopy, which has been used in contemporary battery management systems [12] [13], on the other hand requires extensive experimentation and rest periods. Hence, both methods are unsuitable for real-time battery operation. As a result, substantial research in the last decade has focused on developing data-driven methods for SOH estimation, using for example convolutional neural networks or long-short term memory networks. A recent review [14] identified that in 57.5% of the solutions for SOH estimation use deep learning models. Current, voltage and temperature measurements are most often used as input for the models, while other sensor data are not usually measured. State of the art models for SOH estimation achieve high accuracy with high-quality datasets, but they often fail to perform well in real-life applications. Limitations of existing technologies:

- Measuring high-quality data suitable for real-time SOH estimation
- Real-time collaborative learning over fleet of batteries poorly explored

- Generalization of SOH estimation on variety of batteries, their usage and environmental conditions is limited
- Trustworthy SOH prediction.

In summary, contemporary SOH estimation is dominated by deep learning on current, voltage, and temperature, yet real-time applicability remains constrained by data quality, distribution shift across heterogeneous batteries and usage conditions, and the lack of privacy-preserving fleet-level collaboration. The main challenges are robust real-time data acquisition, federated learning on non-IID fleets, reliable generalization across chemistries and environments, and transparent, explainable predictions acceptable to operators.

One of the goals of the demonstrator is to develop advanced methods for SOH estimation based on different sensors, including a quantum sensor based on Nitrogen Vacancy centres in diamonds. The goal is to improve the prediction model using magnetic field (generated by currents) information in time and frequency domains during the charging and operational processes of the battery.

4.4 Demo 3.3

Power conversion for automotive traction control is a key contributor to the overall efficiency of electric vehicles. To address this challenge, the adoption of state-of-the-art packaging and interconnection technologies for SiC devices will be investigated within this Demo. Building on I&M's modular architecture, developed over several years, this demonstrator will implement a SiC-based power stage suitable for automotive traction applications. The system targets 150 kW nominal power at 800 V. The architecture is composed of several interconnected units:

- Gate driver board: adapting control signals to the requirements of the power stage.
- Power Module: executing the actual power conversion.
- DC-link capacitor: dimensioned and optimised for the specific application.

The main activities include:

- Development and realisation of an automotive power stage in the 150 kW power range, featuring high breakdown voltage capability.
- Design of a modular architecture to support various automotive applications.
- Development and validation of novel packaging solutions for SiC devices.
- Experimental validation on a dedicated test rig.

A flexible and scalable architecture for high-power converters will be proposed, with the option to integrate quantum sensors (Q-sensors) to support innovative and more precise e-motor control algorithms. This approach would represent a significant step forward compared to the current state of the art.

4.5 Demo 3.4

The application of wide bandgap semiconductors to power conversion is key in new developments. Silicon carbide (SiC) inverters are commonly used in high performance and high efficiency applications, but the costs related to this technology are still higher than silicon counterpart. Gallium Nitride (GaN), instead, claims higher performances than SiC with costs comparable to silicon.

Building on I&M's modular architecture, developed over the last several years, the aim of this demo is to design a GaN-based power inverter suitable for light electric vehicles and motor bikes. The target is to obtain 40 kW at 400 V. The architecture is composed out of the following interconnected components:

- A control unit based on automotive microcontroller units, with different computational performances
- A gate driver board, adapting control signals to the ones required to drive the power stage appropriately
- A power stage, performing the actual power conversion
- A DC-link compatible with the application.

This architecture has been developed through EU funded projects: HiPerform (ECSEL Joint Undertaking (JU) under grant agreement No 783174), EVC1000 (EU Research and Innovation programme Horizon2020 under grant agreement No. 824250), HiEfficient (ECSEL Joint Undertaking (JU) under grant agreement no. 101007281), and HiPE (Horizon Europe research and innovation programme under grant agreement No. 101056760). The first three projects helped to define and structuring the architecture, whilst the latter developed a GaN-based inverter for auxiliary drive (2 kW maximum power).

This demo starts from this legacy to extend the power level of the unit and reach the target (40 kW). To achieve this target, the power stage will be redesigned to host multiple transistors in parallel and will use newer devices available on the market. Changes to the gate driver board are also possible to adapt the existing board to the new power stage. Special care will be given to the EMI filter that will be designed and integrated in the final design.

4.6 Demo 3.5

In Demo 3.5, Verum and TU/e are building a low-code Robotic Operating System ROS 2 orchestrator that automatically generates code from formal-method specifications. The formal method technologies enhanced in Cynergy4MIE will be employed in the chosen demonstrator, showcasing ROS2's relevance to automotive and/or advanced robotics applications.

However this Demo will not be covered in detail in this Deliverable because it deals almost completely with software.

4.7 High-bandwidth Current Sensor

With the introduction and advancement of wide-band semiconductors in power converters, the limits on power density and switching frequencies are pushed and expended with every new generation of semiconductors. Although this enhances the application domain and opens door to new technologies and implementation, it also stresses the existing control and components infrastructure that is used in power converters.

One of the subcircuits that is stressed, is the current measurement. Vital for many applications, the increasing switching frequencies also challenge the existing current measurement structures, due to the correlation between the switching frequency and the bandwidth of the current measurement. As

such, switching frequencies in the multi-megahertz range push the limits of the current measurement in the hundreds of megahertz range.

Not only the bandwidth can be a limiting factor. With increasing switching frequency, soft-switching of the semiconductors is essential. Therefore, the direction of the current, especially the zero-crossing of the current, is important. All delay that is present between the actual zero-crossing and the detection of the zero-crossing, either in soft- or hardware, contributes to additional losses and a limitation of the potential of converters. Therefore, also an advanced phase-delay compensation will be added to the current measurement to enhance the overall usability of the current sensor.

To summarize. The key components that will be added to the state-of-the-are in current sensing:

- Current measurement with a bandwidth in the order of hundred of megahertz
- Advanced phase-delay compensation for zero-crossing detection of the current
- Scalable design for wide current range

5 Minimally Invasive Sensors for Efficient, Fail-Safe EV Powertrains (Demo 3.1)

Demo 3.1 is subdivided into two use cases. The first use case, UC3.1.1, focuses on the development of a millimetre-wave torque sensor. The second use case, UC3.1.2, explores approaches for replacing the physical position/speed sensor in the motor control loop. Since it is mostly about using software to replace hardware, this second use case is not covered by this deliverable, which deals with components and sensors.

5.1 UC3.1.1 Torque Sensor Specification

The specifications for the torque sensor are based on the requirements defined in the deliverable D1.3.

5.1.1 Reflectometer - Test Chip (IFAT)

The torque sensor test chips are transceivers for the frequency range around 140 GHz. They are manufactured in Infineon Si-Ge technology. Figure 1 shows a block diagram of the main transceiver version with on-chip antenna. It is based on a mono-static architecture with a single antenna shared for transmitter (TX) and receiver (RX). The circuit contains the 140 GHz signal generation, transmitter and receiver. Analog to digital conversion of the baseband signals, and frequency control of the operating frequency, are not included in this chip and have to be performed externally.

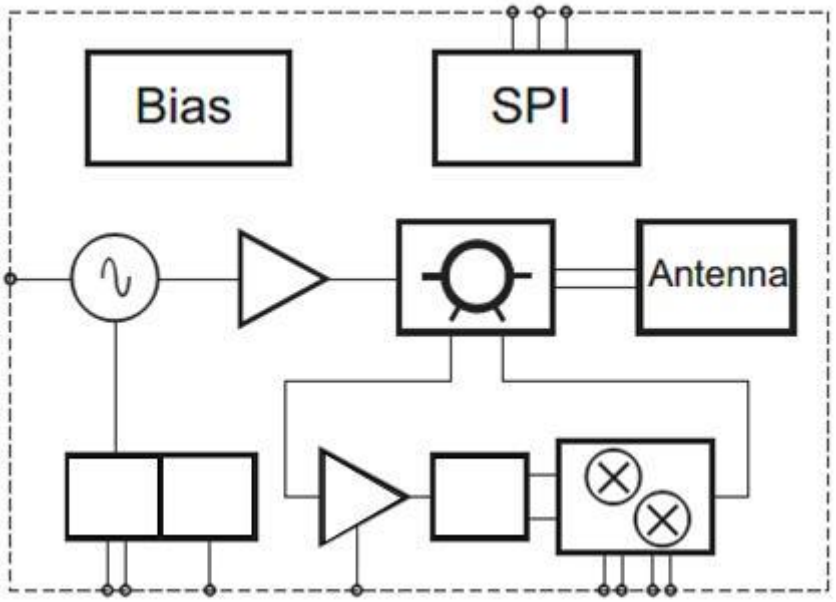

Figure 1: Block diagram of the reflectometer test chip

For the torque sensor application, monostatic sensors have the advantage of providing an identical transmit and receive antenna pattern. On the other hand, the use of a common antenna leads to crosstalk between transmitter and receiver. This results in a high DC offset at the baseband outputs. The required coupler between transmit and receive path of the monostatic sensor also decreases the signal-to-noise ratio.

5.1.2 Test Chip Pad Frame

Pads are aligned on two opposite sides of the chip to be compatible with packages such as PG-TDSO-16. In order to minimize crosstalk, digital signals (SPI, low-frequency divider output) are located on one chip edge, and sensitive signals (tune voltage input and baseband outputs) on the opposite edge.

Several redundant pads for VSS (ground) and VDD are provided. Only a single VDD and VSS connection is sufficient for operating the chip. However, it is recommended to contact two VSS pads and two VDD pads for long-time reliability.

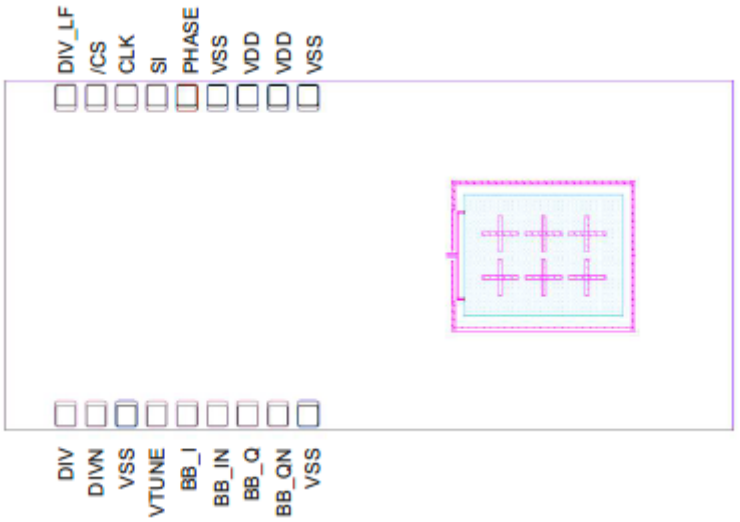

FIGURE 2: PAD FRAME FOR TDSO16 PACKAGE HTTPS://WWW.INFINEON.COM/PACKAGE/PG-TSSOP-16-1

Pin List

The following list gives an overview about the type and function of the different pins of the test chip.

Name	Type	Function	Comment
VSS	Ground	Ground	
VDD	Supply	Supply Voltage	3.3 V ±5%
VTUNE	Analog Input	Tune Voltage	allowed range: 0 V to 5 V
DIV	RF Output*	Non-inverted frequency divider output	f > 1 GHz
DIVN	RF Output*	Inverted frequency divider output	f > 1 GHz
BB I	Analog Output*	Non-inverted inphase baseband output	
BB IN	Analog Output*	Inverted inphase baseband output	
BB Q	Analog Output*	Non-inverted quadrature baseband output	
BB QN	Analog Output*	Inverted quadrature baseband output	

DIV LF	Digital Output	Low-frequency divider output	3.3 V CMOS levels
PHASE	Digital Input	Phase inversion of receiver LO signal	3.3 V CMOS levels
SI	Digital Input	SPI data input	3.3 V CMOS levels
CLK	Digital Input	SPI clock input	3.3 V CMOS levels
CS	Digital Input	SPI chip select (low-active)	3.3 V CMOS levels
TRX	*RF Input/Output*	*Non-inverted receive/transmit input/output*	
TRXN	*RF Input/Output*	*Inverted receive/transmit input/output*	
TX	*RF Output*	*Non-inverted transmit output*	
TXN	*RF Output*	*Inverted transmit output*	
RX	*RF Input*	*Non-inverted receive input*	
RXN	*RF Input*	*Inverted receive input*	

TABLE 2: PIN LIST (*SHORT-CIRCUIT FROM THIS PAD TO GROUND WILL DAMAGE THE CHIP)

Pin Description

- VSS: on-chip ground. All VSS pads are connected on chip. For reliability reasons, it is recommended to connect at least two of the available VSS pads.
- VDD: supply voltage (3.3 V±5%). All VDD pads are connected on chip. For reliability reasons, it is recommended to connect at least two of the available VDD pads.
- VTUNE: tune voltage of the VCO. The allowed voltage range extends from 0 V to 5 V. When this voltage range is not fully used in the application, this will reduce the tuning range.
- DIV, DIVN: differential frequency divider output. Differential output of the high-frequency divider stages, output frequency > 1 GHz. The differential output is designed for an AC coupled external load of 2× 50 Ohm.
- BB I, BB IN: differential baseband output for the inphase signal. This differential interface provides the output signal of the inphase mixer. The outputs are DC coupled, with a DC common-mode voltage determined by the mixer. The baseband interface is intended for use with a high-impedance load (>=10 k Ohm).
- BB Q, BB QN: differential baseband output for the quadrature signal. This differential interface provides the output signal of the quadrature mixer. The outputs are DC coupled, with a DC common-mode voltage determined by the mixer. The baseband interface is intended for use with a high-impedance load (>= 10 kOhm).
- DIV LF: low-frequency divider output. The output of this pin is a CMOS compatible rail-to-rail digital signal.
- PHASE: control input for LO phase inversion. This CMOS compatible digital input controls the phase of the local oscillator signal. Depending on a high or low level at this pin, the LO signal is either inverted or not inverted. This will change the DC offset created by the crosstalk from transmitter to receiver. The signal at this pin has no effect when Bit 2 in Register 9 is set to 1.

- SI: SPI data input. This CMOS compatible digital input receives the SPI data signal. The pad has an on-chip pull-up.
- CLK: SPI clock input. This CMOS compatible digital input receives the SPI clock signal. SPI data are clocked into the device at the falling CLK edge. The pad has an on-chip pull-up.
- CS: SPI chip select input. This CMOS compatible digital input serves as low-active SPI chip select signal. The pad has an on-chip pull-up.
- TRX, TRXN: differential receive/transmit input/output. Test chip versions TRQ3 and TRQ5 are intended to be used with an external antenna.Instead of an on-chip antenna these chips contain a ground/signal/ground/signal/ground RF pad interface. The impedance level for the differential TRX/TRXN signals is 2× 50 Ohm
- TX, TXN: differential transmit output. The chips contains a ground / signal / ground / signal / ground RF pad interface for the transmit signal. The impedance level for the differential TX/TXN signals is 2× 50 Ohm
- RX, RXN: differential receive input. The chip contains a ground/signal/ground/signal/ground RF pad interface for the receive signal. The impedance level for the differential RX/RXN signals is 2× 50 Ohm

5.2 Draft Concept Design

5.2.1 General Description Demo Board

The torque sensor test board is a compact printed circuit board that integrates a 140 GHz or a 60 GHz IQ reflectometer with a PSOC6 microcontroller to provide reliable measurement, local processing, and digital communication. Designed for ease of integration, the board supports common interfaces, includes onboard power regulation, and offers provisions for calibration, firmware updates, and diagnostics.

System Architecture:

The microcontroller manages sensor data acquisition, local filtering, and communication with the host system. The sensor interfaces to the MCU via SPI, and sampling is scheduled through firmware timers. A CAN and GPHSS Interface provides data output. Real-time data acquisition is possible over USB Interface. Optional a programmer interface for PSOC6 microcontroller provides live debugging feature.

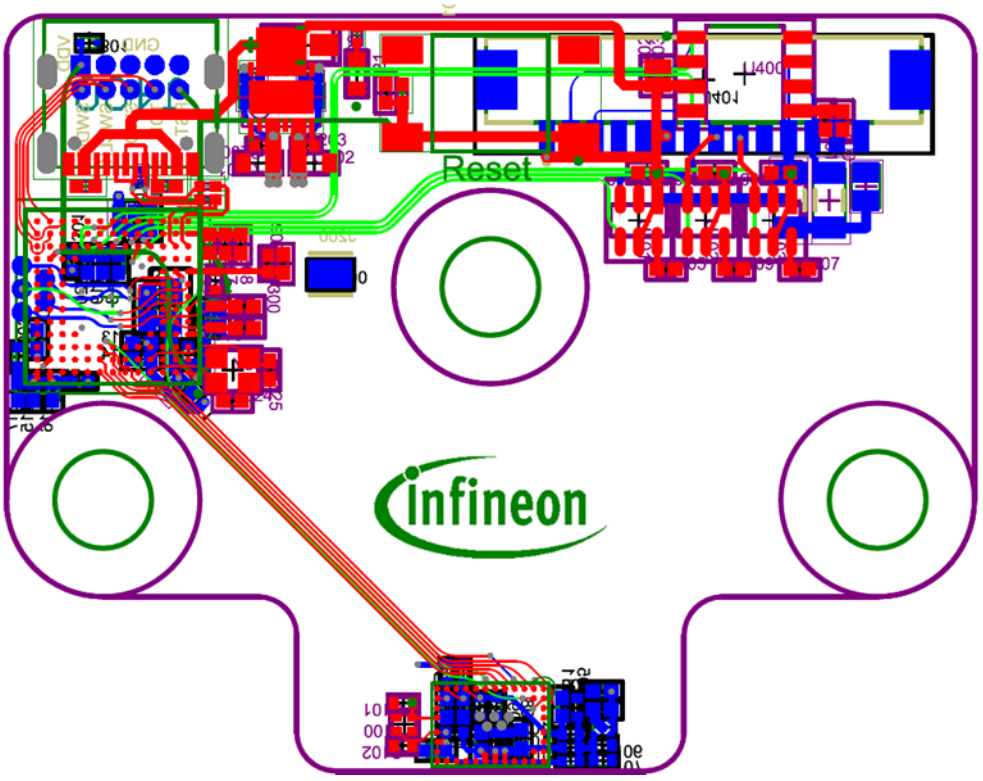

Figure 3: PCB Layout Demo Board

5.3 First Results

The first Test Chip is available as bare die which also was the basis for the measurement set up. The process for packaging is ongoing.

5.3.1 Torque Sensor Test Chip On-Wafer Measurements

On-wafer characterization of torque sensor test chips was performed at 25°C with a 3.3 V supply. Measurements used default register settings unless otherwise noted and cover the MMIC only, excluding the on-chip antenna. In the following figures, the first results of the measurements on the wafer are presented.

Supply Current

The graph below shows the supply current with default settings. The exact value will depend on activated circuit blocks and DAC settings for the amplifiers

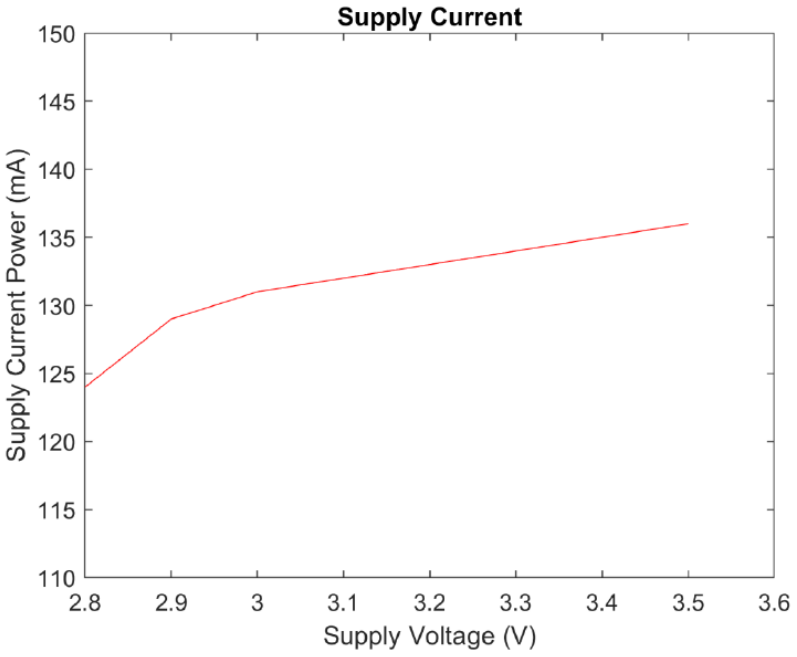

FIGURE 4: SUPPLY CURRENT WITH DEFAULT SETTINGS

Frequency Divider

The graph shows the single-ended output power at the high-frequency divider pin DIVN

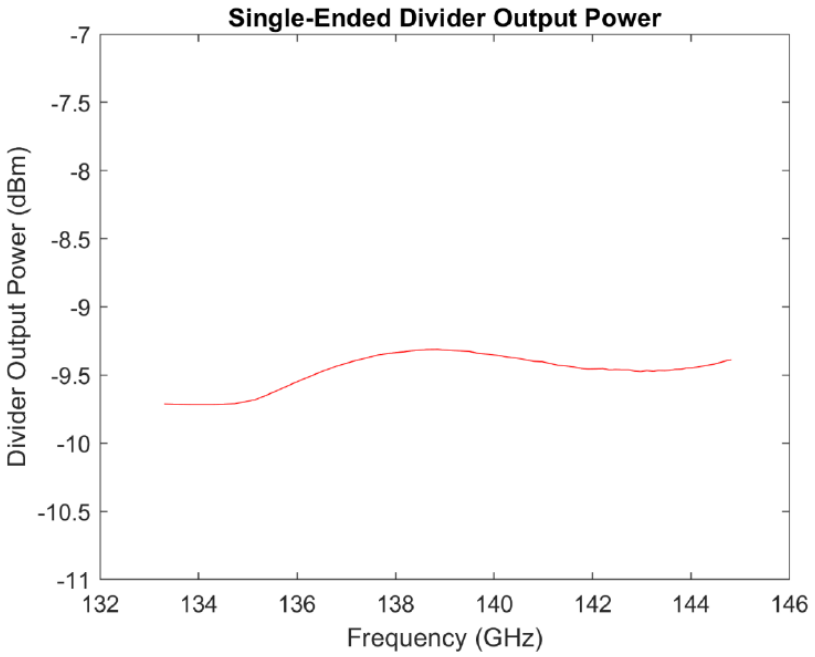

FIGURE 5: SINGLE-ENDED OUTPUT POWER AT THE HIGH-FREQUENCY DIVIDER PIN DIVN

TX Output Power

This graph shows the output power at the antenna port of the MMIC version without on-chip antenna. The TX power amplifier setting at default value. The losses of measurement setup introduce measurement uncertainty.

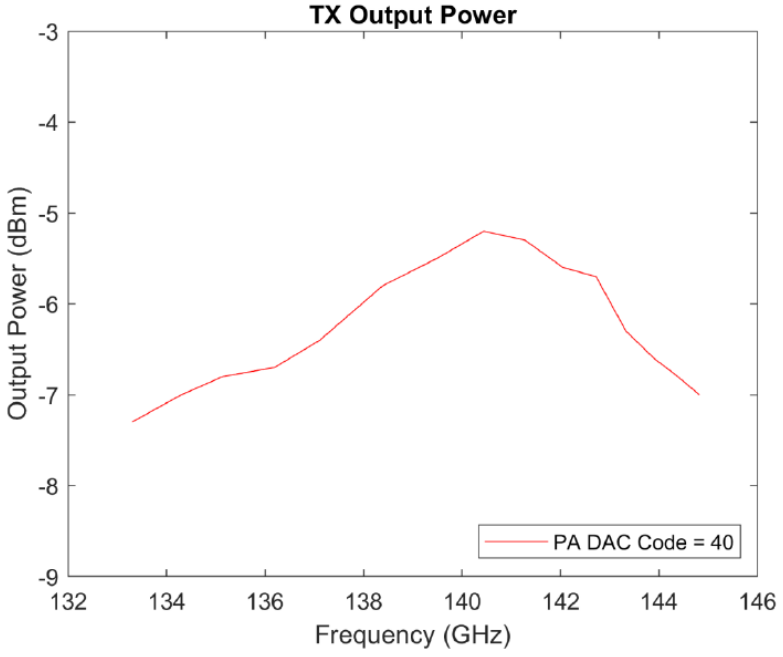

FIGURE 6: OUTPUT POWER AT THE ANTENNA PORT OF THE MMIC VERSION WITHOUT ON-CHIP ANTENNA

Baseband Voltage

The measurement is taken at the single end and also as a differential baseband measurement.

The first graph shows the single-ended baseband voltages. The common-mode voltage is ≈ 2.5 V. The DC offset between non-inverted and inverted baseband signals is caused by TX/RX crosstalk.

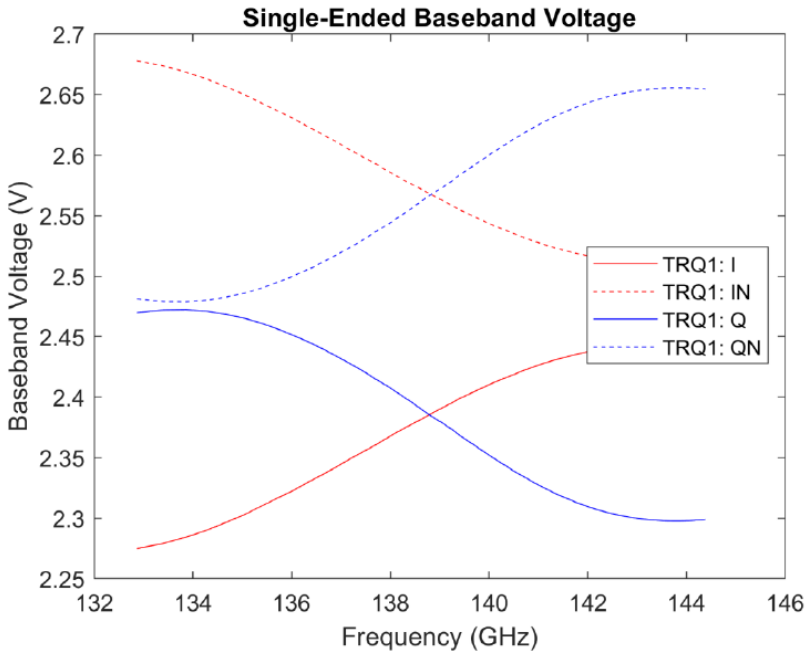

FIGURE 7: SINGLE-ENDED BASEBAND VOLTAGES

The second graph below shows the differential baseband voltages. The DC offset between non-inverted and inverted baseband signals is caused by TX/RX crosstalk.

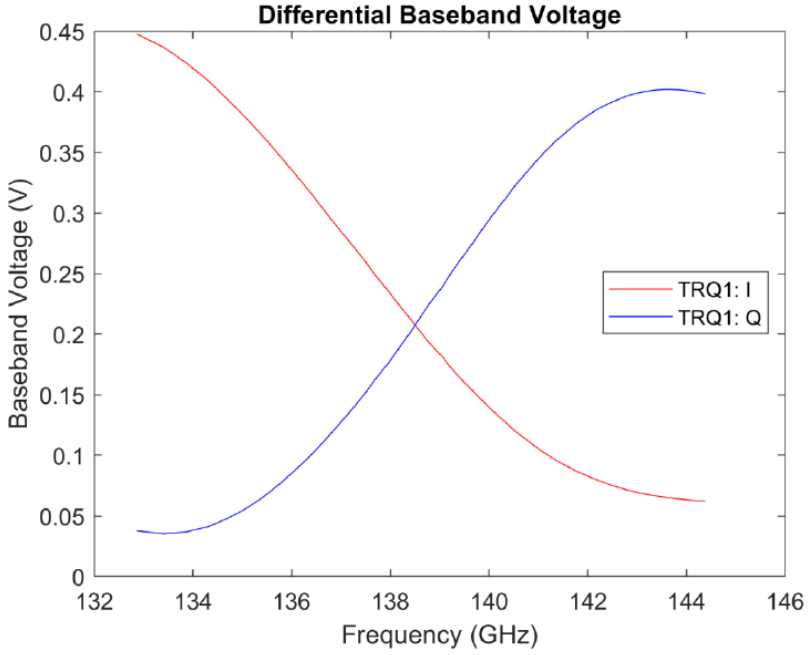

FIGURE 8: DIFFERENTIAL BASEBAND VOLTAGES

5.4 Static and Dynamic Torque Sensor Test-Bench Development (TUG)

5.4.1 Introduction and Motivation

Two test benches are developed by TUG to characterize the system consisting of the radar chip and the passive sensor element of the metamaterial discs, within the mechanical system. The first and smaller set up is called the "Static Set-Up". Its purpose is to gain insight on the behaviour of the sensor system including different metamaterial discs, as well as the mounting of the discs to the shaft and thus the initiation of displacement due to a static torque load. The KPIs to determine with the static set up for the respective metamaterial disc/mounting arrangement are:

- Repeatability
- Hysteresis
- Characteristic Curve
- Signal Temperature drift

The second set up called "Set-up Rotation" is used after the characterization of the static parameters. The assembly consisting of the shaft, the metamaterial discs, and their connection to the shaft is inserted from the static structure into the rotating structure without making any changes to this assembly. This minimizes the changes in the influencing factors that the mechanical periphery has on the measurements in both setups, making them more comparable. The illustration below shows the shaft assembly with the metamaterial discs.

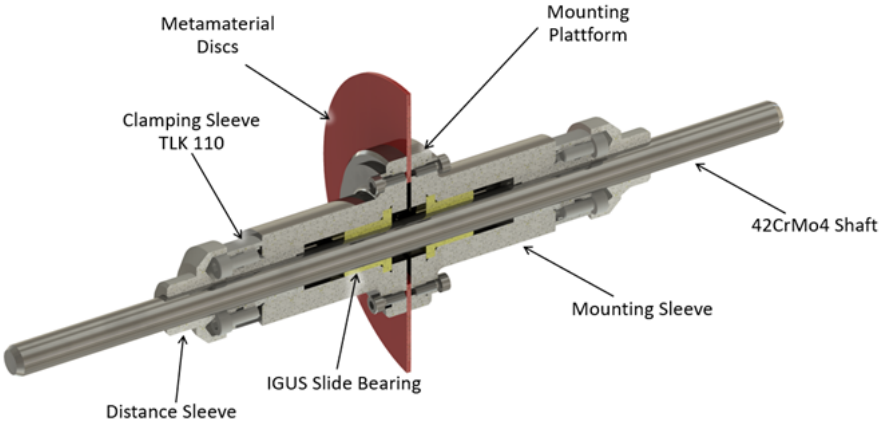

Figure 9: Shaft Assembly including the Metamaterial Discs

Parameters to determine with the "Set-up Rotation" are for example:

- Accuracy (Compared to calibrated reference torque Measurement Shaft)
- Repeatability of the Signal in Rotation
- Dynamic behaviour und changing torque and speed
- Influence of vibration and parasitic forces (e.g.: Bending moment on the shaft)

5.4.2 Static Set-up Design and first Measurements

The main goal of the design of the static set-up was, that the same shaft assembly can be easily switched between the two set-ups, as well as simplicity and the minimization of bending moment on the shaft assembly. Figure 10 below shows the main parts of the assembly.

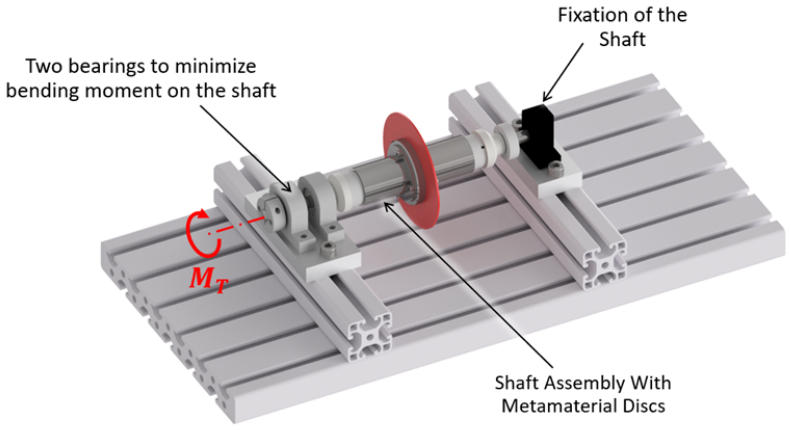

FIGURE 10: STATIC SET-UP OVERVIEW

The torque M_T is achieved via a long lever that is mounted symmetrically in the centre and weights that are hung at defined positions on the lever to achieve the desired torque. Shown below is a first example measurement with this set-up in the form of the characteristic curve showing the relation of the signal to the respective torque including 95% KI intervals. The measurement range was -8 to +8 Nm negative direction D2; positive D1.

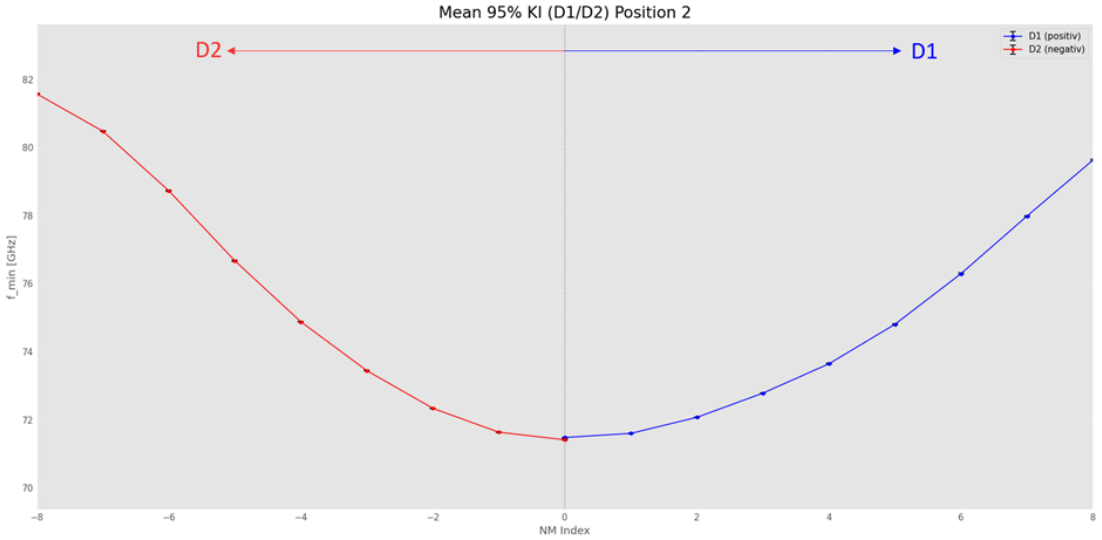

FIGURE 11: CHARACTERISTIC CURVE - FIRST MEASUREMENT WITH THE STATIC-SET UP

The results of the measurement are promising, as the show good reproducibility of the measurement signal and high sensitivity to torque changes in the range outside of +-3 Nm. The low sensitivity in the range around zero is due to the initial alignment of the used metamaterial sample mounted on the shaft and is expected. This set-up thus serves as a vital part in the development of the metamaterial

torque sensor to determine the vital KPI's of different assembly set ups before testing them in a dynamic rotating environment.

5.4.3 Set-up Rotation Design Overview

This setup is designed as a dual-motor test bench for testing various metamaterial discs and radar chips in a dynamic rotating system. A schematic concept overview, showing main components, flow of power and information can be seen in Figure 12.

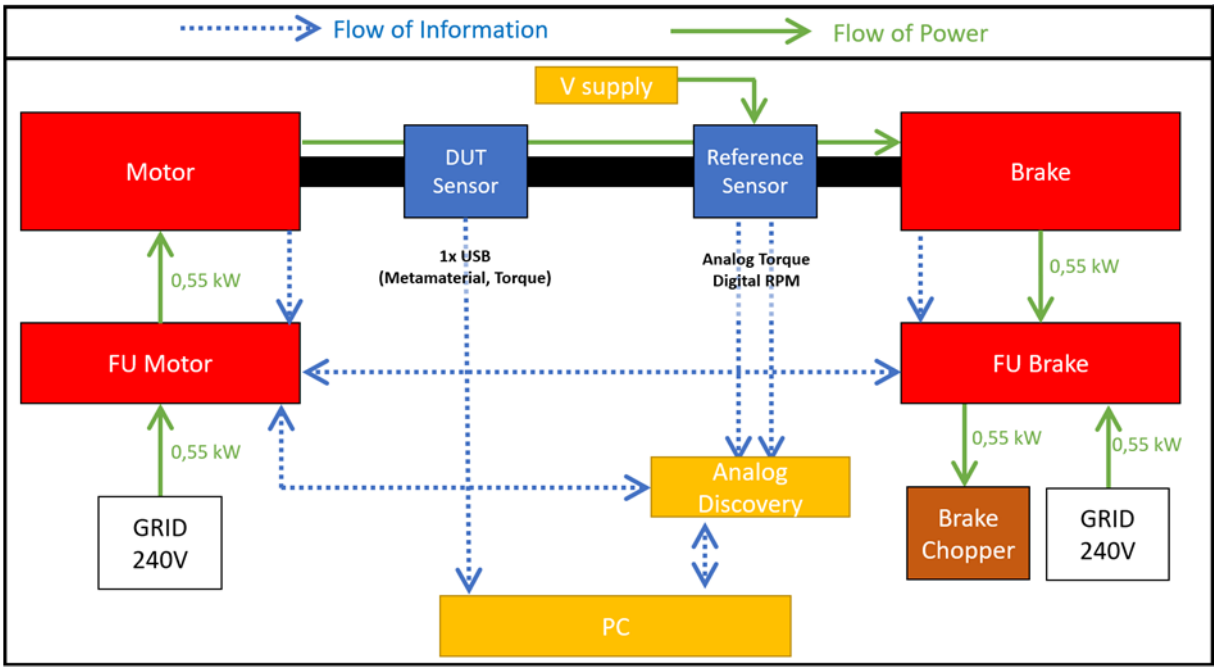

FIGURE 12: SET-UP ROTATION CONCEPT OVERVIEW

The control of the motor and reference sensors is realized via an Analog Discovery 2. Therefore, it is possible to program curves for torque and speed, thus achieving repeatable test conditions for the DUT in the form of the metamaterial torque sensor. The cross section including the shaft and reference sensor is shown in Figure 13. A rotationally symmetrical design was chosen in order to centre the segments as precisely as possible via fits, thereby avoiding parasitic bending moments on the DUT and providing high torsional rigidity.

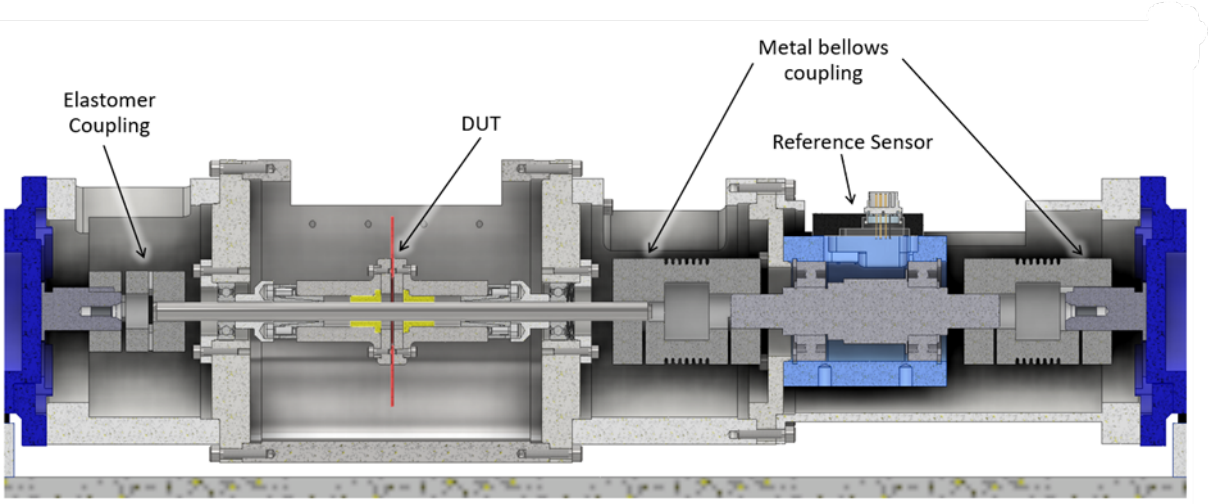

FIGURE 13: CROSS SECTION OF THE SET-UP ROTATION

The integration of the first radar chip and metamaterial disc sample is shown in Figure 14.
"A" shows the mounted sensor and evaluation board on the test bench including a small fan to cool the sensor. "B" shows a close-up of the radar sensor and the used metamaterial discs.

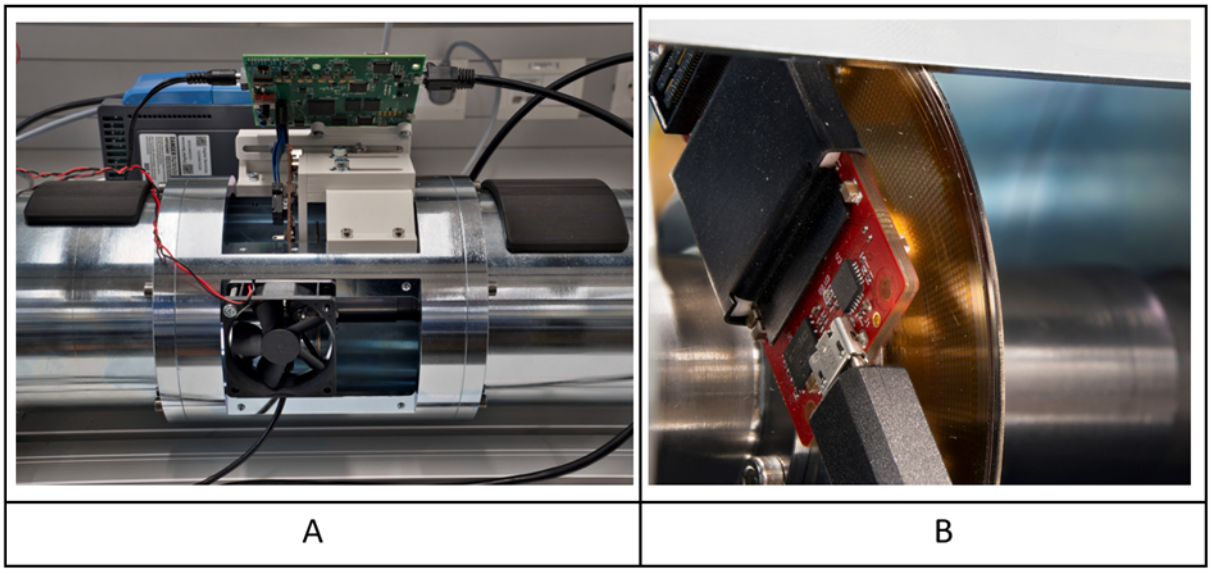

FIGURE 14:
A: Mounted Radar Sensor and Evaluation Board - B: Close-up of the Radar Chip and Metamaterial Target

Initial measurements in rotation have already been taken, and the raw signal from the radar sensor looks promising. In the next steps, the signal will be recorded several times with defined curves on the test bench, and the post-processing of the signal will be optimized. In addition, various metamaterial targets will be tested in addition to the targets initially used, which are made of glass.

6 Modular, High-Performance, Smart Battery for Mobile Machines (Demo 3.2)

6.1 Specification

FAU – Quantum Sensor

Current Battery Management Systems (BMS) typically rely on external sensors to monitor electric currents. However, this external monitoring often lacks the sensitivity and temporal resolution required to detect very small or rapid internal changes. To optimize charging cycles and ensure safety in high-performance mobile machine applications, there is a critical need for sensors that can probe the state of the battery cell with high precision. FAU addresses this challenge by introducing a minimally invasive sensor solution based on Nitrogen Vacancy (NV) centers in diamond. This quantum sensing technology allows for precise measurement of magnetic fields. The motivation is to provide the BMS with high-fidelity, real-time internal data, potentially enabling more aggressive yet safe utilization of the battery's capacity.

6.2 Identification of Components

FAU – Quantum Sensor

The quantum sensor is comprised of multiple components: A fiber-connected sensorhead, a fiber-optic and electric transmission line, and an opto-electronic control unit. The control unit is then connected to the user.

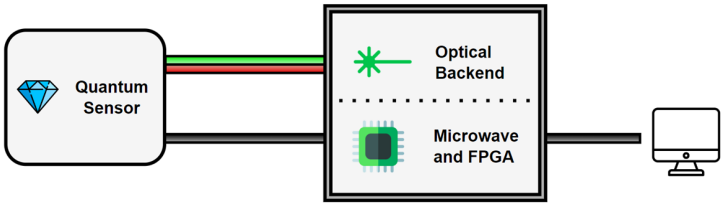

Figure 15: Components of the Quantum Sensor: Fiber-based sensorhead, electrical and optical connection to the electro-optical backend and connection to user

EDI – Quantum Sensor Electronics

The electronics section includes the analogue components and digital programmable logic. The analogue electronics module handles the control of the microwave field and the acquisition of the light intensity measurements, and is reused R&D. It is designed as a custom PCB made up of commercial integrated circuits. Most of the digital logic is contained within a custom ASIC that implements a System on Chip (SoC) which includes a RISC-V processor core, embedded programmable logic core and specialised components for quantum sensor measurements.

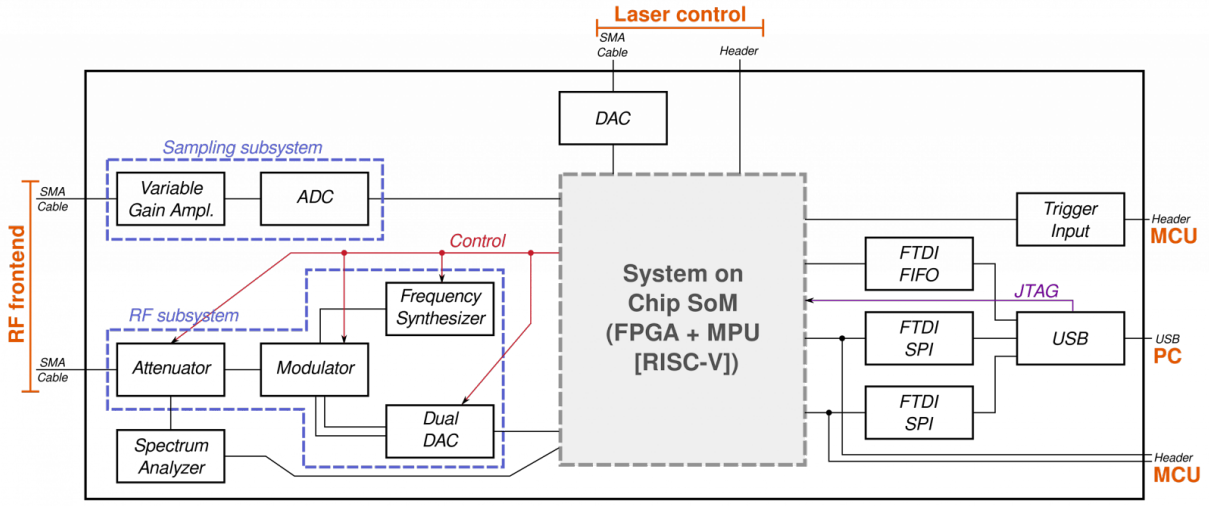

FIGURE 16: OVERVIEW OF THE QUANTUM SENSOR ELECTRONICS

6.3 Draft Concept Design

FAU – Quantum Sensor

The core sensing element of the quantum sensor consists of a diamond enriched with Nitrogen Vacancy centers, attached to the tip of an optical fiber. To maximize the photon collection efficiency, FAU built an optimized micro-lens system at the fiber tip. This optical chain is responsible for delivering the green excitation laser light (520 nm) to the diamond and collecting the red fluorescence response (650-780 nm). Another constraint is the delivery of microwave radiation to the sensing volume to enable Optically Detected Magnetic Resonance (ODMR). Therefore, the sensor includes a miniaturized loop-shaped microwave antenna integrated in close proximity to the diamond tip to drive the spin transitions.

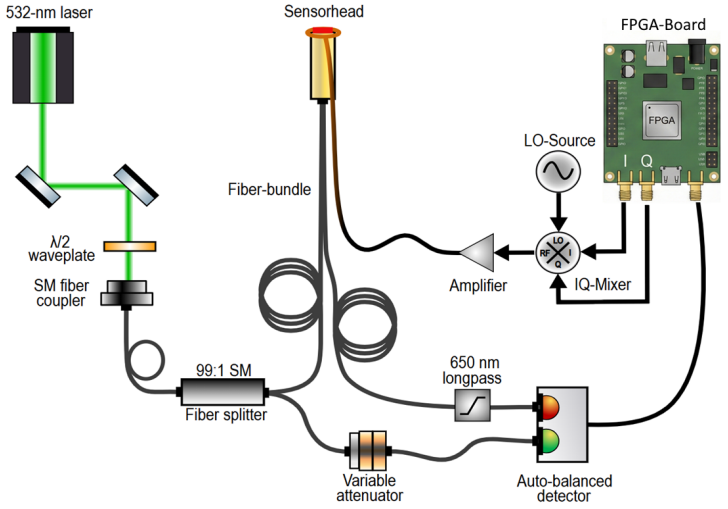

FIGURE 17: DETAILED DESIGN CONCEPT FOR THE FIBERIZED QUANTUM SENSOR. MINIATURIZED SENSOR HEAD WITH DIAMOND AND LOOP ANTENNA, AND AN ELABORATE OPTICAL BACKEND FOR CREATING THE EXCITATION SIGNAL AND FLUORESCENCE COLLECTION, AS WELL AS AN FPGA BASED ELECTRICAL BACKEND

EDI – Quantum Sensor Electronics

Some of the components implemented in digital logic include systems for controlling the analogue electronics modules, processing blocks that handle calculations necessary for quantum sensor measurements, interfacing components for communication with the user and a custom data compression accelerator. If required, additional components can also be implemented using the embedded programmable logic core, which could, for example, add support for different ICs to be used in the analogue section.

At the core of the generic measurement architecture is the event router – a user-configurable interconnect for event (essentially trigger) signals. Every component features an event input and output, which respectively trigger the action performed by the component and signal its completion. By routing the event signals, the user is able to chain the individual components in a manner required by the particular measurement method. An array of configurable delay lines enables precise timing of the performed actions, especially useful for defining custom pulse-based measurement protocols.

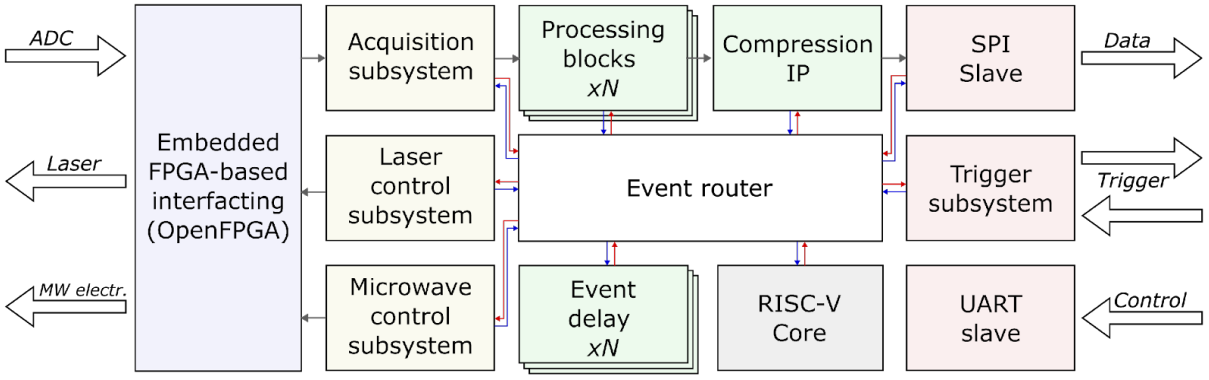

FIGURE 18: ARCHITECTURE OF THE MEASUREMENT SYSTEM DIGITAL LOGIC

SAL – Silicon Austria Labs

In collaboration with FAU and EDI, SAL focuses on Li-ion battery characterization using a state-of-the-art quantum sensor developed at FAU. This sensor offers a sensitivity of 150 pT/√(Hz), enabling the detection of extremely weak magnetic fields. The sensor was applied to investigate current distributions within Li-ion battery cells, revealing detailed maps of the internal magnetic field. The experimental setup uses a motorized stage to generate a full map of the magnetic field. To ensure accurate measurements, the sensor head was placed in a zero-Gauss chamber, shielding it from external magnetic fields.

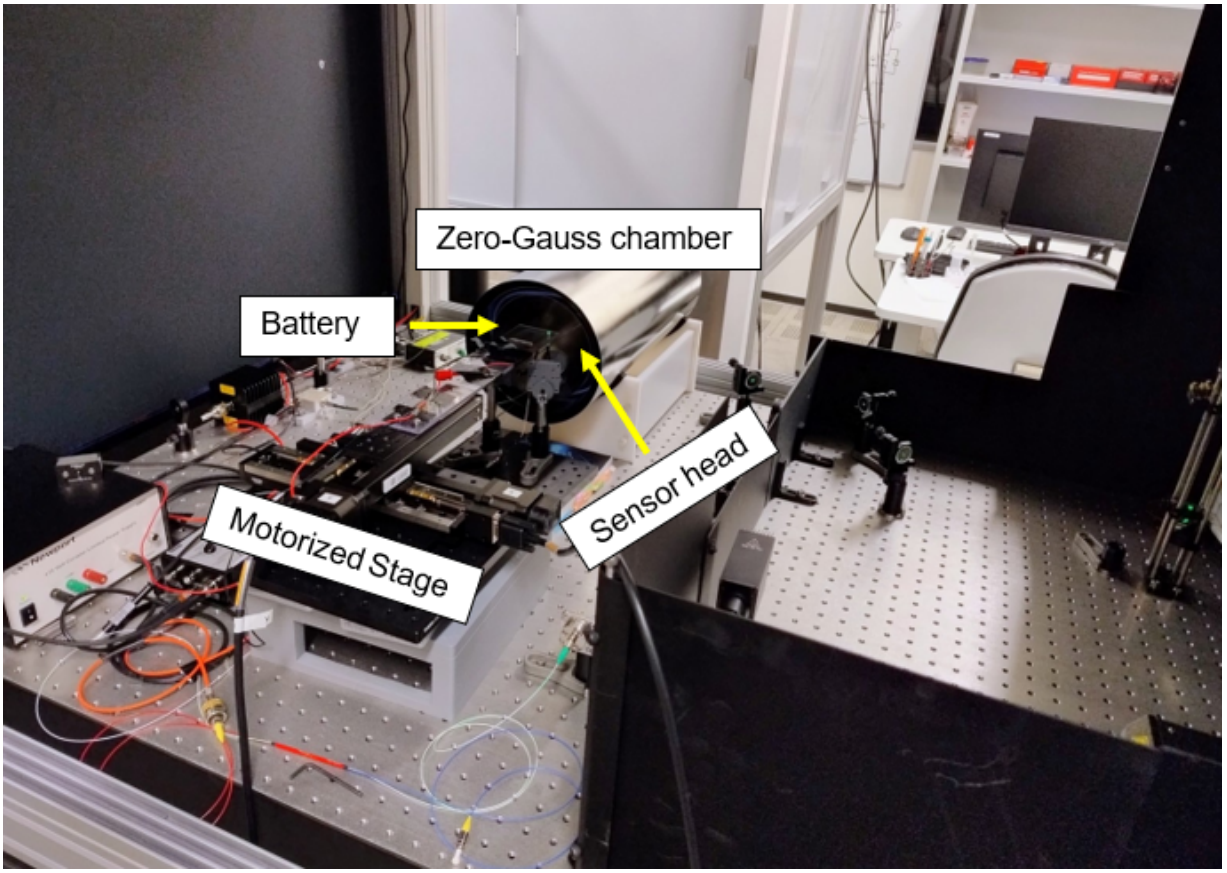

FIGURE 19: EXPERIMENTAL SETUP SHOWING THE QUANTUM SENSOR HEAD PLACED INSIDE A ZERO-GAUSS CHAMBER, AND A MOTORIZED STAGE IN FAU'S LABORATORIES.

6.4 First Results

FAU – Quantum Sensor

In collaboration with SAL, FAU has conducted first battery measurements, measuring the local magnetic field of pouch battery cells during charging and discharging. These measurements have shown that the quantum sensor is able to determine the small magnetic fields that the currents inside of the battery generate during charging/discharging processes. Measuring this local current distributions can for example help in understanding SoH degradation due to local changes in the battery.

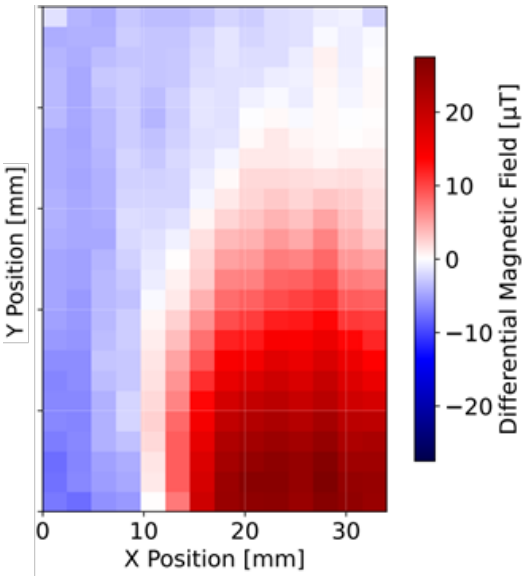

Figure 20: Magnetic field of a pouch-cell, measured in collaboration with SAL in FAU's laboratories

EDI – Quantum Sensor Electronics

EDI has verified major parts of the generic measurement architecture on an FPGA development kit. It is currently capable of performing Optically Detected Magnetic Resonance (ODMR) measurements and is being extended with lock-in amplification support and capabilities for pulse-based measurement methods.

SAL – Silicon Austria Labs

In collaboration with FAU, SAL experimentally validated a quantum-sensor-based setup for Li-ion battery characterization through the induced magnetic fields, enabling localized hotspot detection and SoC and SoH estimation. Ongoing research is being carried out to further improve the methodology and improve estimation accuracy.

7 SiC Power Inverter for EVs @ 150 kW / 800 V (Demo 3.3)

7.1 Specification

The specifications for the silicon carbide (SiC)–based power stage based on the requirements identified in section 9 of the deliverable D1.3. The power stage is designed for operation on an 800 V-class DC bus, with an allowable input voltage range from 520 V to 850 V. It is specified to deliver a continuous output power of 80 kW under steady-state operation (S1) at 800 V and cos(ϕ) = 0.9 and a maximum output power of 160 kW for short-time operation (S3), defined as 10-second intervals repeated up to 10 times within 10 minutes under the same electrical conditions. In three-phase operation, the power stage shall be capable of supplying a continuous phase current of 100 A rms and a maximum phase current of 200 A rms under short-time conditions consistent with the defined S3 duty cycle.

From a performance standpoint, the power stage is specified to achieve an efficiency greater than 96% and to operate with a variable switching frequency in the range of 8 kHz to 20 kHz, enabled by the use of SiC MOSFET technology. The adoption of SiC devices, together with advanced packaging and cooling concepts, supports a target power density exceeding 50 kW/l, considering the power stage elements only (power modules, DC-link capacitors, gate drivers, and cooling system).

The power stage architecture is specified to be modular and scalable, enabling adaptation to different automotive traction applications and facilitating compact integration within vehicle platforms.

From an electrical perspective, the use of SiC MOSFET technology imposes strict constraints on the commutation loop inductance in order to safely enable fast switching operation. Excessive parasitic inductance may result in increased voltage overshoot and device overstress. Consequently, the power stage specification includes the requirement for a low-inductance power layout, enabling high slew rates within safe operating limits.

7.2 Identification of Components

7.2.1 DC-Link Capacitors

The DC-link capacitor represents one of the most critical elements of the power stage and accounts for a significant portion of the overall mass. Its primary function is to provide the power stage with the required electrical energy during high-frequency switching events. In order to support fast switching operation of the SiC MOSFETs, the DC-link and power devices must be arranged in a low-inductance configuration. For this reason, a dedicated DC-link capacitor module has been analyzed and evaluated to meet the electrical and layout constraints imposed by high-speed SiC operation.

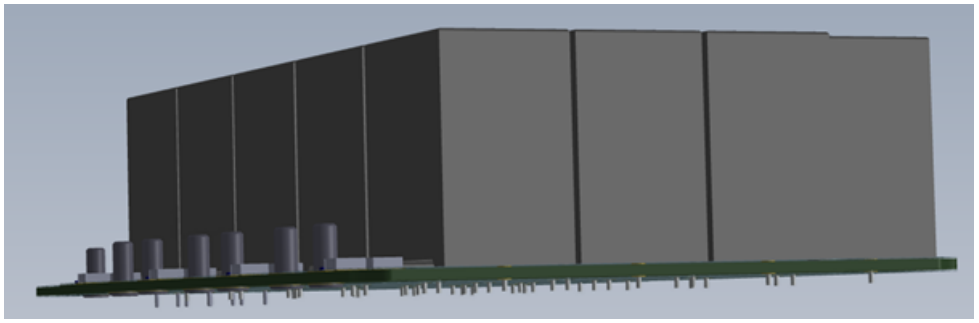

Figure 21: Custom DC-Link Capacitor Board

This design can be seen in Figure 21. Instead of adopting a conventional laminated busbar solution, the design is based on a thick copper printed circuit board. This choice enables the integration of multiple electrical and mechanical functions into a single component while relying on widely available and well-established manufacturing processes. As a result, the overall system complexity is reduced, assembly is simplified and cost efficiency is improved without compromising electrical performance. The unit features a total capacity of 140uF.

7.2.2 Liquid Cooler

In order to enable operation at the maximum achievable output power, effective thermal management of all heat-generating components is required. To this end, a direct liquid-cooling solution has been developed for the power modules. The resulting cooler concept is illustrated in Figure 22.

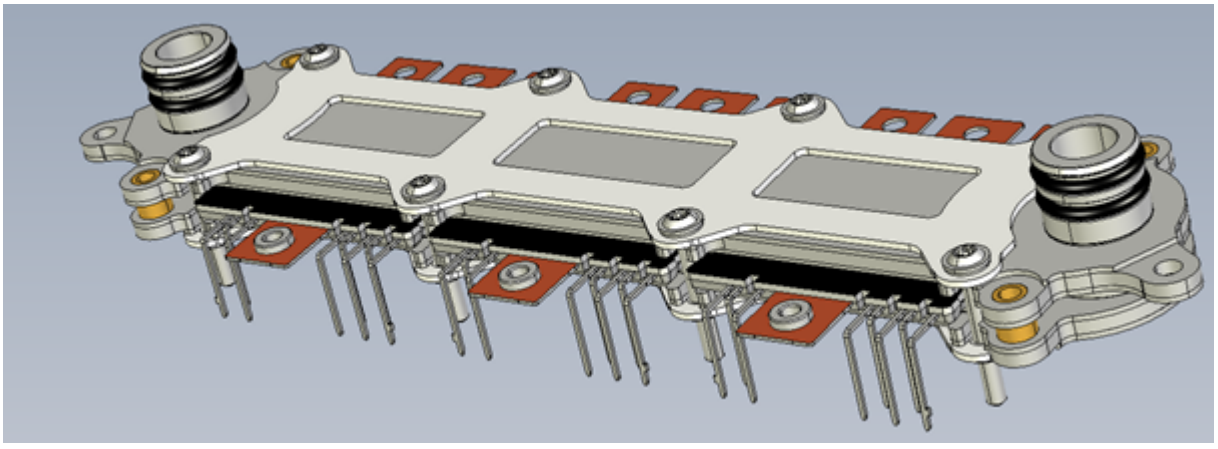

Figure 22: Power Modules cooling system

The coolant enters the system through a single inlet and is subsequently distributed into two parallel flow paths, ensuring that both top and bottom baseplates of the power modules are exposed to coolant at comparable inlet temperatures. To maximize the heat exchange between the modules' baseplates and the cooler, thermal pads are inserted at the interfaces. In addition, internal bypass channels are incorporated to promote coolant circulation across the cooler volume, contributing to a more uniform thermal distribution and supporting heat removal. Sealing of the cooling circuit is achieved using O-rings. To ensure leak-free operation, a dedicated pressure test is required as part of the validation process.

7.2.3 Power-Modules

The commutation cell represents the fundamental building block of the power stage. For a standard three-phase traction application, two controlled switches are required per motor phase, resulting in a total of six power switching devices. In the proposed architecture, the power stage is implemented using three identical half-bridge modules, providing a modular and scalable solution well suited for automotive traction systems.

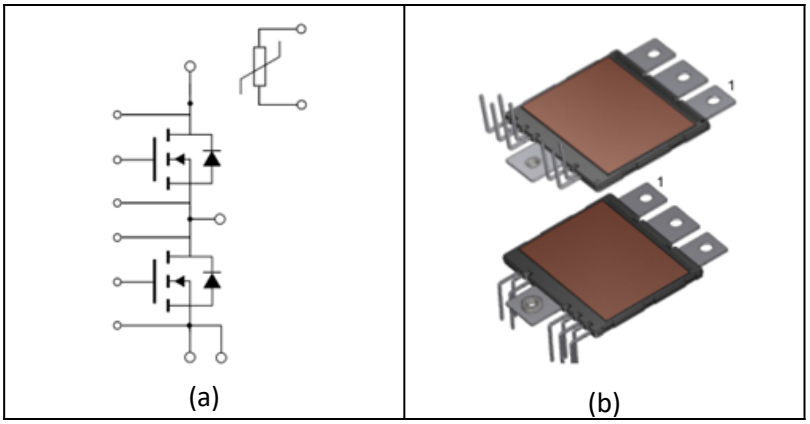

FIGURE 23: ELECTRICAL SCHEMATIC (A) AND 3D VIEW (B) OF ADDH900120W3 POWER MODULE

The selected power devices are the ST ACEPACK™ Gemini ADDH900120W3 module, integrating 1200 V-class SiC MOSFETs optimized for high-voltage and high-power operation. The module is designed to support high phase currents in the 600 A class, making it suitable for traction power stages operating in the 150 kW range on 800 V DC platforms. The SiC MOSFETs are characterized by a typical Rdson of 1.86 mΩ, very low switching energy and a maximum junction temperature of 175 °C, enabling high-efficiency operation under both continuous and transient load conditions. The compact module layout results in a very low stray inductance, typically around 5 nH, which is a key enabler for high-speed switching and reduced voltage overshoot.

On the thermal side, the ACEPACK™ Gemini package features double-sided cooling through exposed copper interfaces, providing excellent thermal performance and supporting high power density operation. The module is AQG 324 qualified and offers an insulation capability of 4.2 kV DC, ensuring compliance with automotive traction inverter requirements.

These characteristics make the selected module well suited for high-efficiency traction applications, providing a robust and scalable foundation for the proposed SiC-based power stage.

7.3 Draft Concept Design

The proposed SiC power stage adopts a modular, multi-board architecture consisting of an isolated gate driver board based on Infineon EiceDRIVER™ isolated gate driver ICs, an interface board designed to map the power module pinout onto a standardized mechanical and electrical interface, and a dedicated expansion board integrating the required sensing functions.

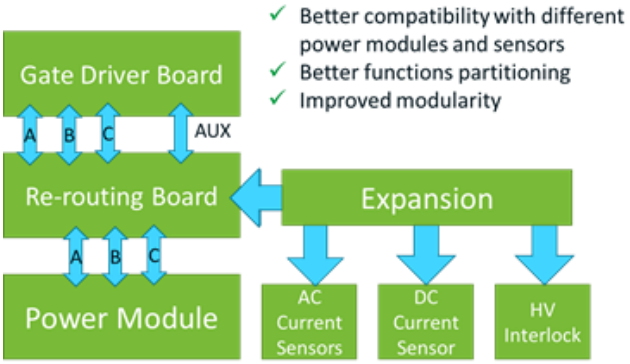

Figure 24: Modular design concept

This stacked board arrangement is designed to accommodate ST-I SiC power modules, with three modules configured in a half-bridge topology. The resulting power assembly is intended to operate with liquid cooling to ensure adequate thermal performance at high power levels. The architectural layout is specifically optimized to minimize parasitic inductances, with particular focus on the interconnections between the power modules and the DC-link capacitors, which is a critical aspect for high-speed SiC switching operation.

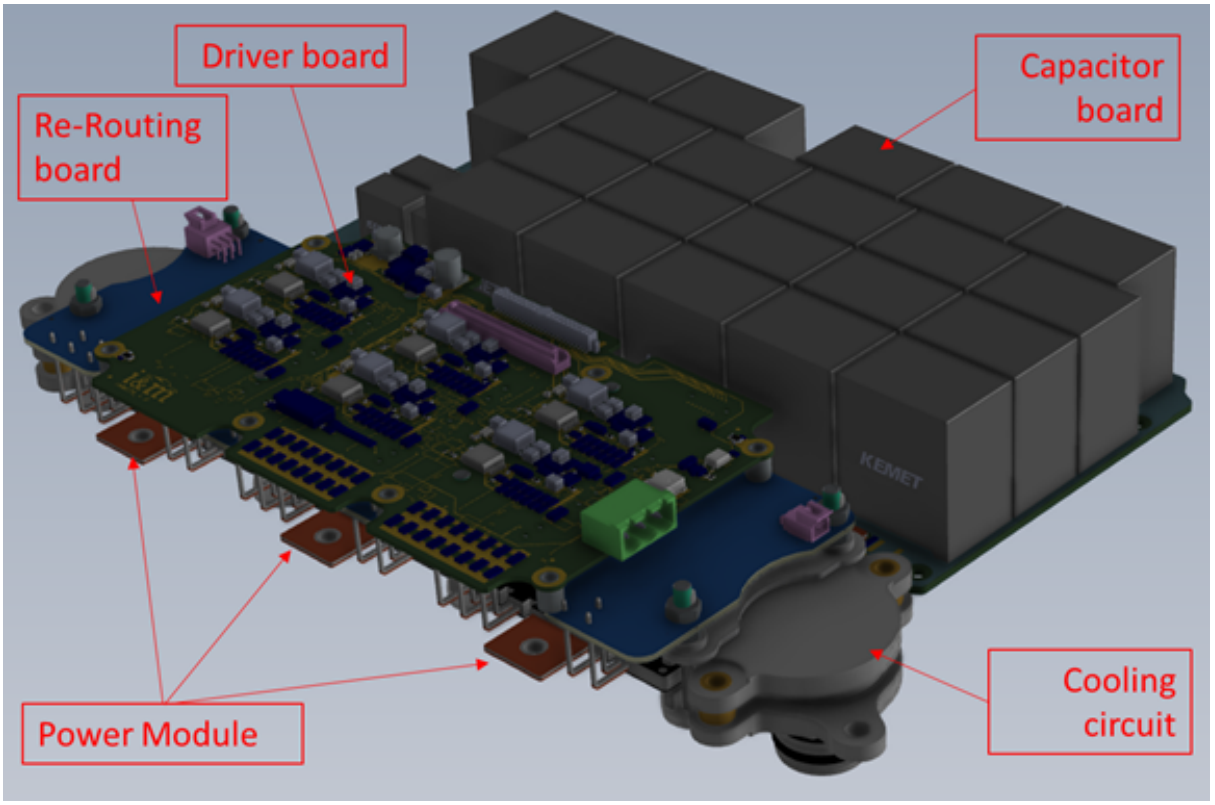

Figure 25: Modular Design Realization

7.4 First Results

As a first validation activity, an impedance characterization of the DC-link capacitor board was performed in order to compare the expected electrical behavior with experimental measurements. The objective of this activity was to assess the accuracy of the design assumptions and to verify the effectiveness of the low-inductance layout adopted for the power stage. The characterization was carried out using a Vector Network Analyzer (VNA), enabling the measurement of the complex impedance of the DC-link capacitor board over a wide frequency range. The measurement setup was specifically configured to capture parasitic effects associated with the capacitor arrangement, interconnections, and printed circuit board layout, which are critical parameters for high-speed SiC switching operation.

Measured impedance data were then compared with the predicted impedance profiles derived from the design models and component datasheets. The comparison focused in particular on the impedance magnitude and phase trends at high frequencies, where parasitic inductance and equivalent series resistance (ESR) dominate the DC-link behavior.

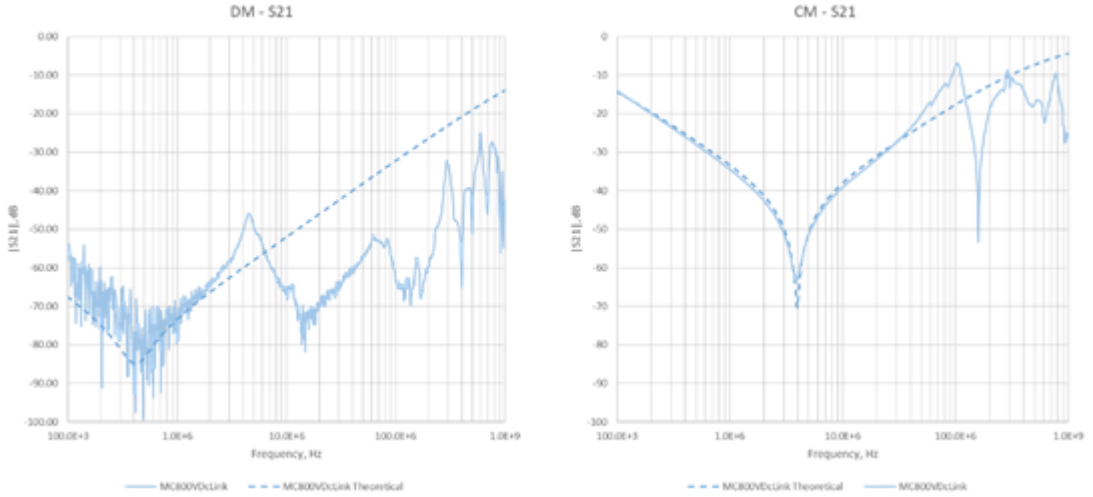

FIGURE 26: COMPARISON BETWEEN SIMULATED AND MEASURED DC-LINK IMPEDANCE

The results show a good agreement between simulated and measured impedance characteristics, confirming that the implemented DC-link capacitor board meets the targeted low-inductance design objectives. Minor deviations observed at higher frequencies are attributed to measurement setup parasitics and manufacturing tolerances and will be further investigated in subsequent development phases.

These initial results validate the chosen DC-link architecture and provide confidence in the electrical performance of the power stage, forming a solid basis for further integration and high-power switching tests.

8 Sensor-Enabled GaN Power Inverter for LEVs / Bikes @ 40 kW / 400 V (Demo 3.4)

8.1 Specification

The power inverter shall be developed as a next-generation automotive traction inverter making use of commercially available discrete gallium-nitride (GaN) power transistors, selected to target automotive applications, with particular emphasis on light electric vehicles (LEVs) and electric motorbikes. The expected output power is 40 kW (peak).

The inverter will be designed to operate correctly at DC-link voltage range between 350 V and 450 V. The inverter shall be compatible with high-frequency switching operation, with a maximum switching frequency of at least 30 kHz, in order to enable reduced passive component size, improved current control bandwidth, and lower acoustic noise. Motor control shall be based on a field-oriented control (FOC) strategy.

Thermal management shall ensure that the inverter is capable of delivering its full electrical performance, including both continuous and S2 peak current operation, for coolant inlet temperatures up to 65 °C. Within this specified coolant temperature range, the inverter shall operate without any thermal derating, ensuring consistent performance even under elevated ambient or vehicle operating conditions.

From a performance perspective, the inverter design aims at achieving a target peak efficiency of at least 96 % under nominal operating conditions. Furthermore, the mechanical and electrical integration of the inverter shall be optimized to reach a minimum power density of 50 kW/L, excluding external cooling infrastructure, thereby supporting compact vehicle integration and weight reduction.

Due to the presence of WBG semiconductors, characterized by steep commutation edges on both voltage and current, the inverter design will also cover the design of an appropriate EMI filter to make the unit compatible with CISPR norms.

This report focuses on the studies performed to extract the specifications to lead the following design phases.

8.2 Identification of Components

8.2.1 Hardware Architecture

The inverter architecture is composed of multiple interacting units to allow design reuse and enable scalability of a given solution.

Figure 27 presents the inverter architecture employed in this project. The proposed design is based on the modular inverter architecture originally developed at I&M and has been adapted to support a broad range of application scenarios. In order to minimize the engineering effort associated with redesigning the inverter for different operational requirements, the overall system is partitioned into four distinct and functionally independent subsystems:

1. the control board,

2. the gate-driver subsystem,
3. the power stage, and
4. the dc-link.

The separation of the inverter into these subsystems enables a high degree of modularity and design flexibility. This modular approach allows individual subsystems to be modified, upgraded, or replaced independently, without requiring a complete redesign of the inverter. Consequently, the hardware platform can be efficiently scaled and adapted to a variety of applications by altering only the subsystems directly impacted by the new specifications, thereby reducing development time and increasing overall system versatility.

Control board and gate drivers have already been developed in the HiPE project timeframe (101056760) and will be only partially adapted to the new power stage. Within the Cynergy4MIE project we will focus on the power stage and on the dc-link.

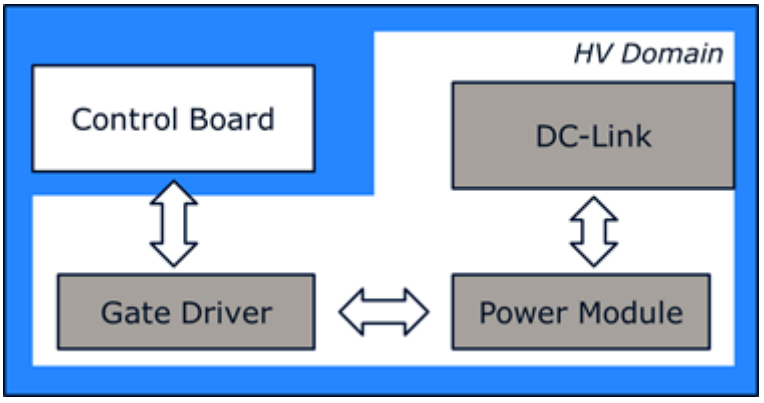

FIGURE 27: HARDWARE ARCHITECTURE

8.2.2 Software Architecture

Software architecture provides a high-level abstraction of a system by defining its principal structural components and the interactions among them. In the context of automotive embedded systems, the software architecture establishes a structured framework for organizing the software of an Electronic Control Unit (ECU) in a modular, scalable, and maintainable manner.

The automotive embedded software architecture is required to define the overall organization of the ECU software while structuring it into horizontal layers in order to reduce development time and associated costs. A key objective of this layered organization is to decouple the application software (ASW) from the underlying hardware (HW) through the introduction of a Basic Software (BSW) layer. This approach enables hardware-independent application development and promotes the standardization of software interfaces exposed to the ASW. Furthermore, the architecture is designed to enhance the reusability and interchangeability of software components, encompassing both BSW and ASW modules.

No further details will be discussed in this Deliverable, as Software will be developed in WP4.

8.3 Draft Concept Design

One of the most critical points for a new inverter is the design of the high-voltage subsystem, i.e., the DC-link and the power stage. In this project a special care has to be devoted to the electromagnetic emissions and this is strictly related to the way the transistors switch. For these reasons, we followed this approach:

1. We developed a digital twin of the power stage, based on previously developed designs and real measurements
2. We used the model to estimate both the stress the power transistor is experiencing during operation and the amount of EM noise generated by the unit
3. We draw some considerations that will guide the following design steps (both on the circuit and on the layout point of view).

The simulations have been developed in the Qspice environment, due to its flexibility in handling SPICE models and higher-level components developed in C++. Nevertheless, this software is free, making it possible to develop very complex model without the need for paying an expensive license.

8.3.1 The Model

Developing a complex model as a three-phase inverter is not straightforward and can require lots of effort [1] [2]. Thanks to the advent of Qspice, a free software from Qorvo, some of the complexities have been removed by the integration of a native capability to model and simulate high level objects in C++.

To study the transistor commutations and the EM noise generated the model is the same and it is visualized in Figure 28. From this model it's possible to identify the three-phase bridge (upper right) corner, the motor windings (lower right), and the battery with the DC-link (lower left). Even if not detailed, or complete, this model is good enough to extract indications for our design.

All the models exhibit some parasitic elements typically not available from the datasheets of the different components. The model has been then populated with values coming from our previous design with similar characteristics.

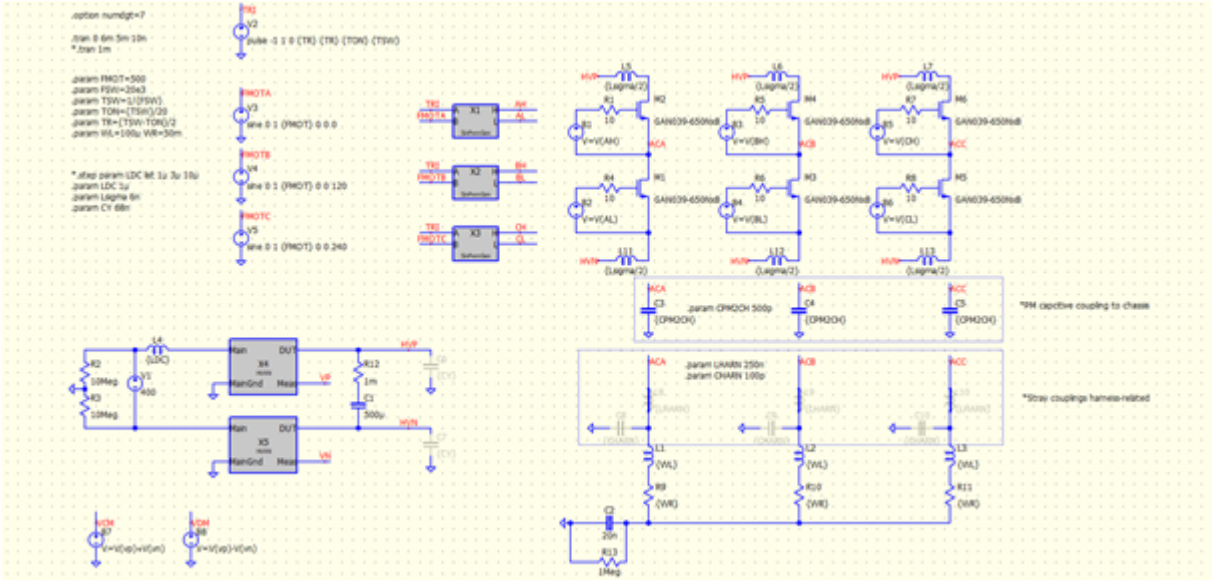

FIGURE 28: QSPICE MODEL OF A THREE-PHASE INVERTER

Qspice allows to generate a SPICE model from the data and the graphs reported on a MOSFET datasheet. Starting from the one of Nexperia GaN014 (not yet released) and GaN039 [3] it is possible to exploit the *Model generator* utility to get an object that mimic the real one.

From the simulations performed it is possible to estimate:

- The voltage overshoot the power device will experience during its turn-off commutation, and
- A high level estimation of the EM noise the converter will generate due to the fast on and off transitions

8.3.2 Voltage Overshoot

To estimate the maximum *overvoltage* allowed, we have to exploit the differential characteristics of an inductor

$$di/dt=\Delta V/L$$

The current slew rate (di/dt) can be either measured or estimated by the simulation model. Looking at the transistor turn-on (Figure 29), it is possible to measure about 18 A/ns. Since the maximum operating voltage is 450 V and the breakdown voltage for these components is 650 V, we can calculate the maximum stray inductance allowed in the DC-loop:

$$L_{dc} \leq \Delta V / (di/dt) = (200\ V) / (18\ A/ns) = 11\ nH$$

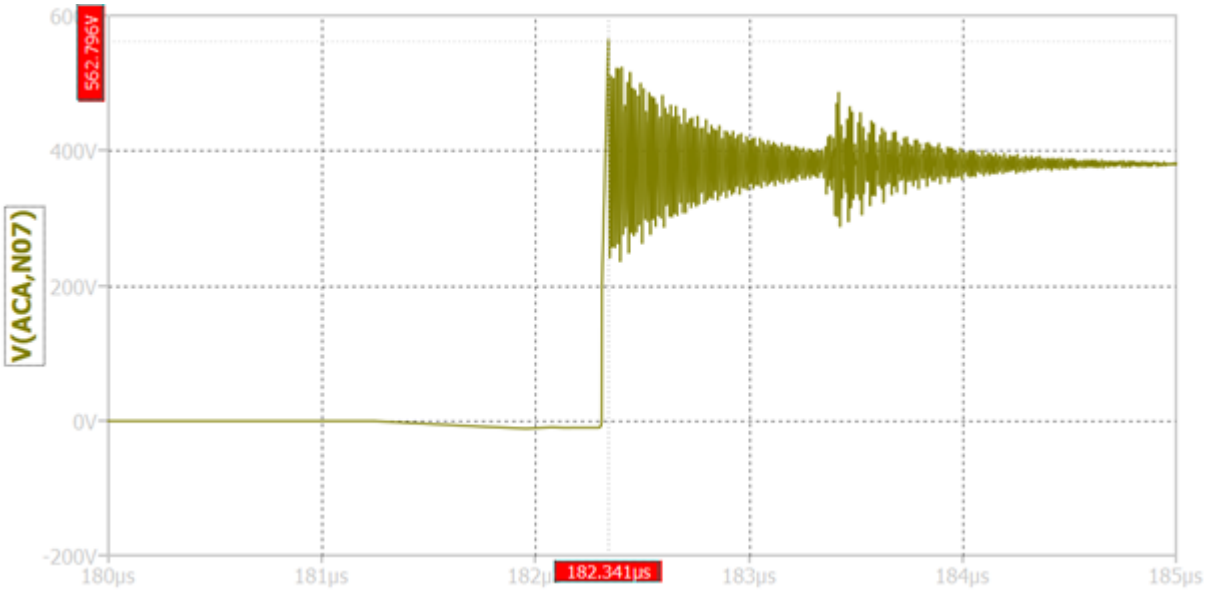

FIGURE 29: TRANSISTOR TURN-ON SIMULATION. THE VOLTAGE OVERSHOOT REMAINS BELOW 200 V AS CALCULATED

To achieve this result, it is important to study a good layout, but also to choose the proper components. Indeed, the typical film capacitors available on the market suitable for the application are prismatic blocks from multiple vendors with stray inductance in the order of 10-15 nH each, because of their physical dimensions. Multiple devices in parallel will improve this value, but the introduction of multiple devices in parallel does not take into account the stray parameters of the PCB used to interconnect them. Indeed, part of the advantage of having multiple capacitors in parallel will be jeopardized by the stray inductance introduced by the PCB connection. This leads to the introduction of a dc-link capacitor composed of multiple devices with multiple technologies:

- Bulky, high capacity film capacitors, suitable to handle the current requested by the load
- Small, low inductance ceramic capacitors, suitable to provide a low-inductive path to the current during commutations

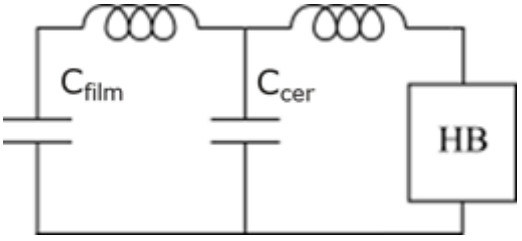

FIGURE 30: DC-LINK NETWORK

Based on these preliminary analyses and considerations the design phase has started and next section will provide some insights about the progresses.

8.3.3 Electromagnetic Interference

Starting from the system simulations performed with the model described in the previous sections, it was possible to estimate the harmonic contents generated by the inverter this is the starting point to

investigate different filtering solutions and thus to optimize the final design. Figure 31 reports the decomposition of the noise at the *high-voltage artificial network* (HVAN) in CM and DM. It is possible to see the predominance of CM noise in the range of interest. The presence of the PWM at 20kHz is clear and all the harmonics are shown Moreover it is evident there is a resonance around 20 MHz to be investigated.

Another important finding got with this approach is to estimate the current flowing towards two important units: the motor and the Y-capacitors (Figure 32). High frequency currents through the motors can wear out the winding insulation and the bearings. For this reason, have an estimation of the currents expected and of their spectrum can be crucial to evaluate different materials and solutions to build an electric motor.

A similar approach can be applied for the Y-capacitors. The advent of wide band-gap semiconductor worsened the slew rates during transitions, increasing the amount of current generated as CM noise. This current will close through the Y-capacitors to avoid polluting the other electronics subsystems in the vehicle, but these capacitors have an *equivalent series resistance* (ESR) that convert the current flowing through it into heat and this heat shall be manageable by the device chosen. Hence thanks to this analysis it is possible to find the proper device(s) to be used to both filter the noise and withstand the heat generated [4].

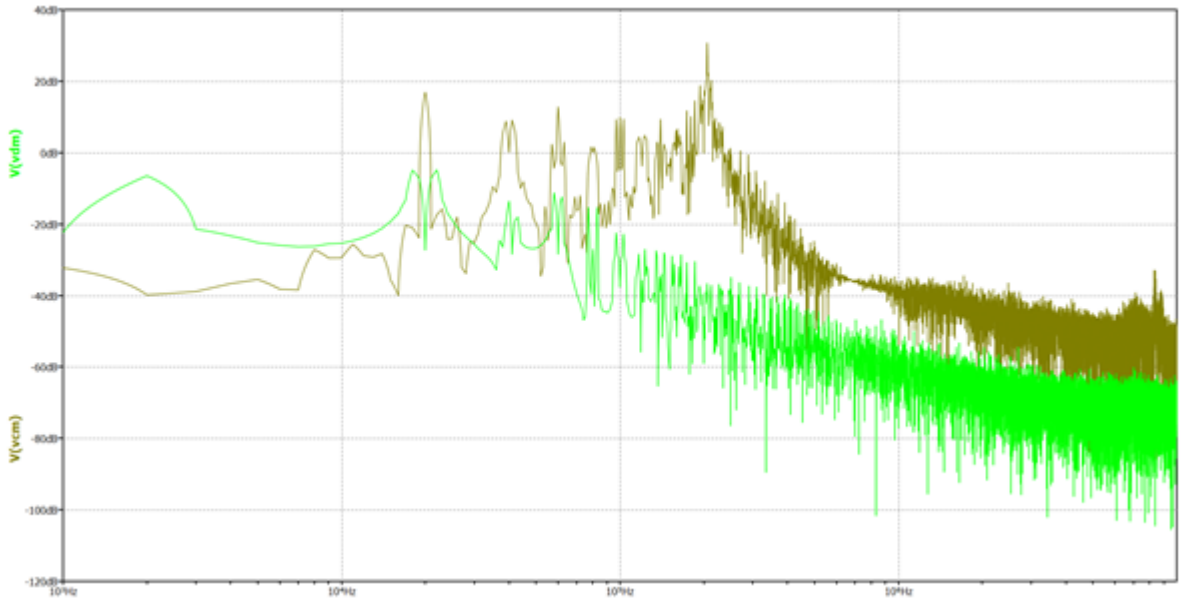

FIGURE 31: CM AND DM NOISE ESTIMATED

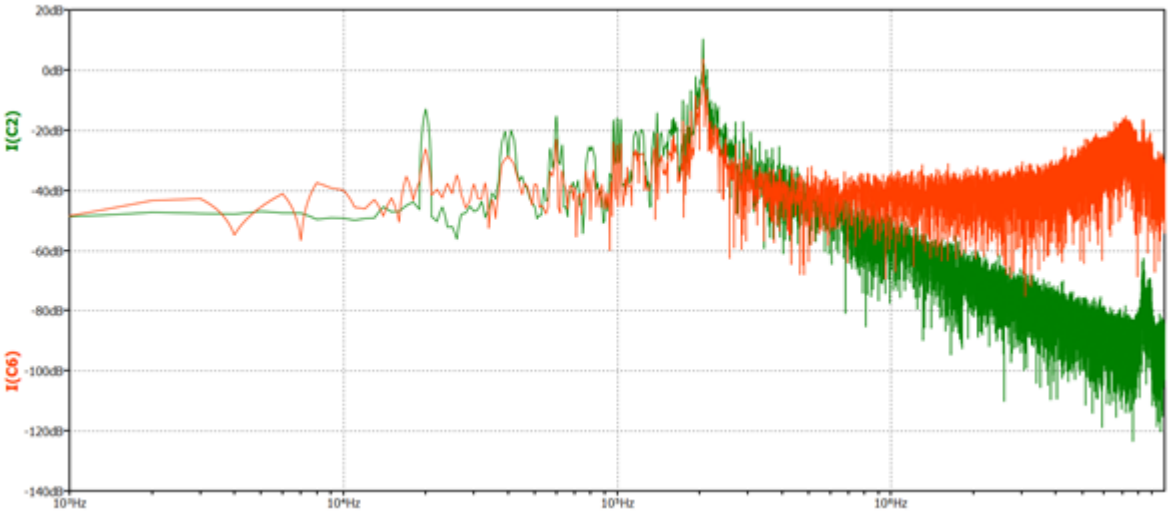

FIGURE 32: SPECTRUM OF THE CURRENT INJECTED THROUGH THE MOTOR (GREEN) AND THROUGH THE Y-CAPS (RED)

8.4 First Results

From the study performed on our simulation models, we derived several design considerations that are included in the design of the power stage, the DC-link, and the preliminary draft of the EMI filter.

8.4.1 Power Stage

The power stage shall provide a peak output power of 40kW in the worst case, i.e., at 350 V, hence the maximum output peak current is given by

$$I_{out} \geq 2/\sqrt{3} \cdot P / V_{DC} = 132 \text{ A}$$

corresponding to an RMS current of 93.3 A.

The power devices under investigation are two from Nexperia:

- GAN039-650NTB, a 33-mΩ GaN cascode transistor able to drive up to 58 A continuously
- GAN014-650NTCA, a 12-mΩ GaN cascode transistor able to drive up to 120 A continuously (experimental device, for this reason we want to keep the compatibility to both chips)

Both these devices are available on bottom- and top-side cooling versions. We opted for the top-side cooled version, since it has been proven very effective in heat extraction achieving best in class figures with respect to other competitor solutions [5].

From the maximum continuous current they can carry, it is evident that both of them are not enough to provide the current required, especially if switching losses are added. For these reasons the idea is to consider a configuration with multiple devices in parallel. Finding the right number of devices to be put in parallel is not easy, since requires the exact evaluation of switching losses and conduction losses in multiple operating points. Considering that both are temperature dependent values, the analysis requires an iterative approach based on simulation software. Our choice was to use an internally developed tool called SimPLE [6] to address this analysis.

The design exploration was done configuring a virtual control unit where it is possible to make parametric the number of devices but also the kind of device can vary. Each configuration has been exposed to an ambient temperature of 65° C cooled with a liquid set at the same temperature. Power losses and junction temperatures were calculated at three switching frequencies, i.e., 10kHz, 20kHz, and 30kHz. Figure 33 and Figure 34 show the results of this analysis.

Amongst the six different power stage configurations, only one is not compatible with the application requirements. Indeed, using 2 x GAN039 does not guarantee to not pass the maximum junction temperature allowed for these devices. The other configurations are fine from this point of view.

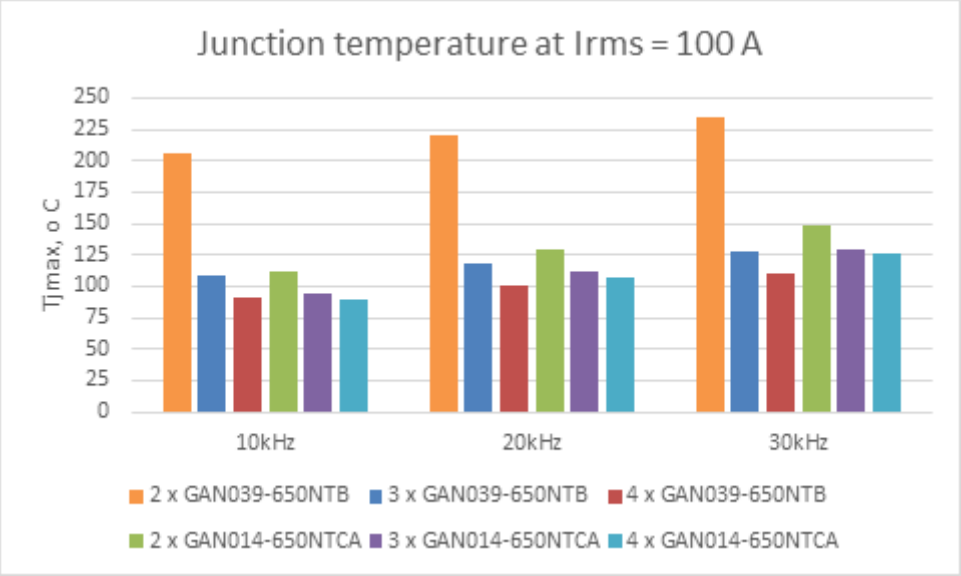

FIGURE 33: MAXIMUM JUNCTION TEMPERATURE OF DIFFERENT POWER STAGE CONFIGURATIONS

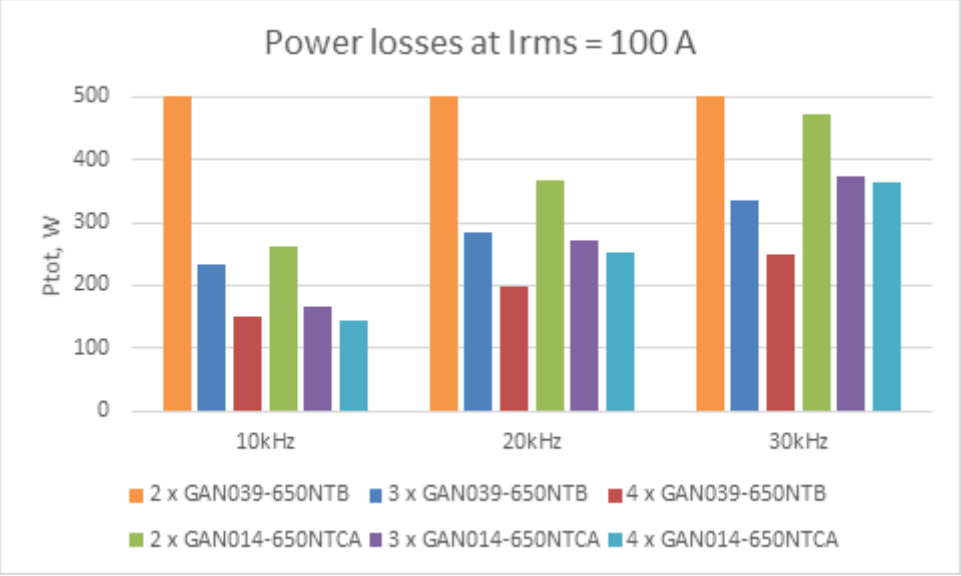

FIGURE 34: TOTAL LOSSES OF DIFFERENT POWER STAGE CONFIGURATIONS

Focusing on power losses (Figure 34), we notice there is another configuration fairly less efficient compared to the others (2 x GAN014), then three configurations have similar performances (i.e., 3xGAN039, 3xGAN014, and 4xGAN014) and one outperforms the others (4xGAN039). Further considerations are possible splitting the loss contribution between conduction (Figure 35) and switching (Figure 36). From these data, the conduction losses are reduced accordingly to the number of devices in parallel as expected, whilst switching losses are not increasing dramatically with the number of chips. This probably because the capacitance increase given by the chips in parallel is partially compensated by the current reduction with a net result of maintaining rather constant the switching losses with the number of devices in parallel.

On the other side, switching losses are highly dependent from the device chosen. The explanation comes from the characteristics of the GAN014 transistor: to improve its ability to drain current, the

size of the die has been significantly increased, with the side effect of increasing also all the capacitive couplings. The result is a much higher current capability at the cost of higher switching losses. Hence, in this application where the maximum switching frequency required is 30kHz, the best solution is to use 4 GAN039 devices in parallel to achieve the best efficiency.

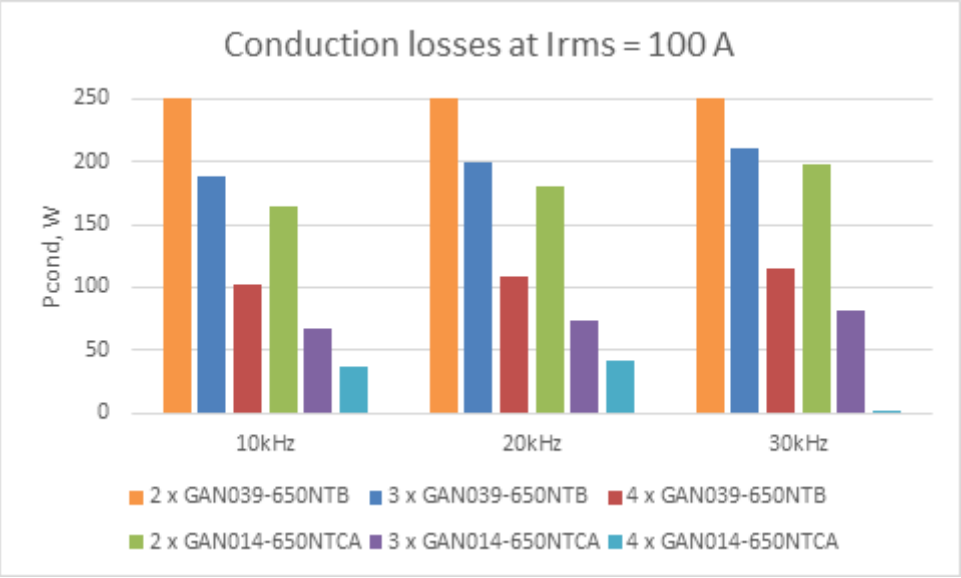

FIGURE 35: CONDUCTION LOSSES OF DIFFERENT POWER STAGE CONFIGURATIONS

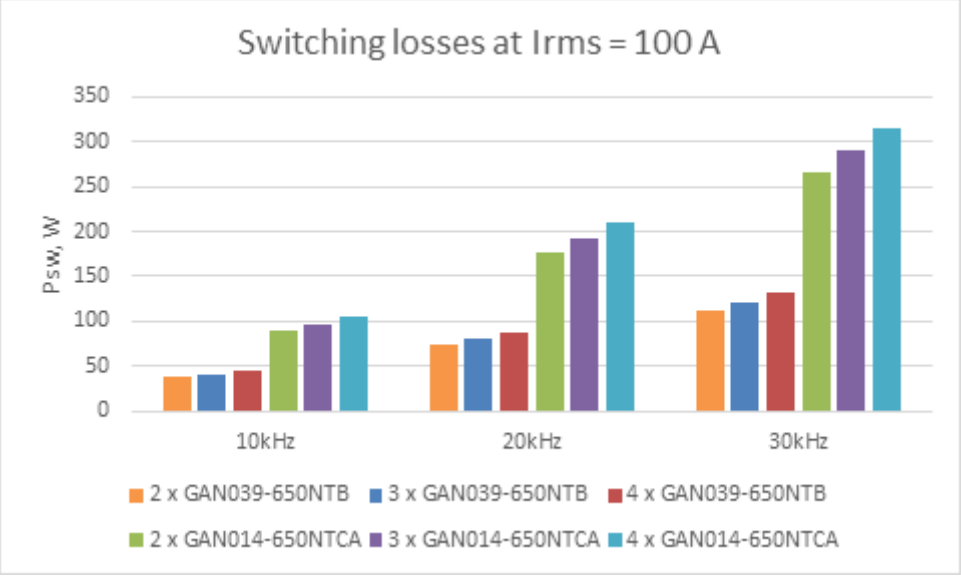

FIGURE 36: SWITCHING LOSSES OF DIFFERENT POWER STAGE CONFIGURATIONS

8.4.2 DC-Link

The dc-link is typically size to accomplish voltage ripple on input and handle the AC current it will experience. In this discussion we also introduce another design criteria, based on the impedance it exhibits to the transistors during the commutations, since GaN devices are very susceptible to the stray inductance present in the DC-loop.

8.4.2.1 Voltage Ripple

The first criterion to size a DC-link is to analyse the voltage ripple. Literature [7] suggests the minimum capacitance required can be obtained by the following formula

$$C\_min = 2 \cdot \max |C \cdot (\Delta V\_3 + \Delta V\_4)| / V\_ripple$$

where $C \cdot (\Delta V\_3 + \Delta V\_4)$ is a 3-D plot displayed in [7], whose maximum is about 0.001; while V_ripple is the maximum ripple allowed on the application. Limiting this value to ± 20V we get

$$C\_min = 2 \cdot (0.001F \cdot V) / (40\ V) = 50\ \mu F$$

This is the first constraint for the capacitor bank.

8.4.2.2 Current handling

Looking to the RMS current the DC-link will have to withstand, literature [8] states its dependency from the phase current I_N, the modulation index M, and power factor cos(ϕ), using this formula

$$I\_(C,rms) = I\_(N,rms) \cdot sqrt \{ 2\ M [\sqrt{3} / (4\pi) + \cos^2(\phi) \cdot (\sqrt{3}/\pi - (9/16)\ M] \}$$

Using the values for this application, the maximum rms current through the capacitors is then

$$I\_(C,rms,max) = 132\ A / \sqrt{2} \cdot 0.65 = 60.7\ A$$

An example of commercial film capacitors suitable for this application are the one from Yageo's C4AU series (Table 3). The choice of this series is given by the operating voltage. Indeed, these devices are compatible with -450 even at high ambient temperatures.

P/N: C4AUJBW5-	Cnom, µF	Vnom, V	Irms, A	ESR, mΩ	ESL, nH
-450M3PJ	45	700	27.6	2.5	14
-560M3PJ	56	700	23.2	4.0	13
-700M3PJ	70	700	27.8	3.3	15

TABLE 3: SELECTED CAPACITORS FROM YAGEO'S CA4U SERIES

Depending on the device chosen, from the capacitance point of view a single device or two are compatible with the application, but the current requirement obliges to go for three devices in parallel. Among the three the selection will be made using the considerations on the DC-loop impedance described in the next section.

8.4.2.3 DC-Loop Impedance

The dc-link has to be designed to have a low impedance for all the frequencies generated in the circuit. Since the highest frequency generated in a power converter is given by the rise/fall time of the power transistors, given the GaN devices provided by Nexperia [3], characterized by a slew-rate of 20V/ns (switch-on) and 45V/ns (switch-off), the maximum generated frequency is given by [9].

$$BW\_max = 0.35 / t\_rise = 0.35 / (\Delta V/SR) = 0.35 / (400 / 45)\ ns = \sim 40\ MHz$$

Film capacitors are not good at frequencies above 1MHz. For this reason, the dc-link designed for this application has been based on a hybrid architecture, combining different capacitor technologies.

Figure 37 shows the impedance of a film capacitor (green line). Due to the stray inductance, above few megahertz their impedance is becoming too high. For this reason, some ceramic capacitors were installed close to the power transistors (orange line). A preliminary estimation of the combined impedance is shown in Figure 37 (blue line), where only the capacitors are considered (stray inductance introduced by the PCB are neglected at this stage, but they will be included and measured in the characterization phase).

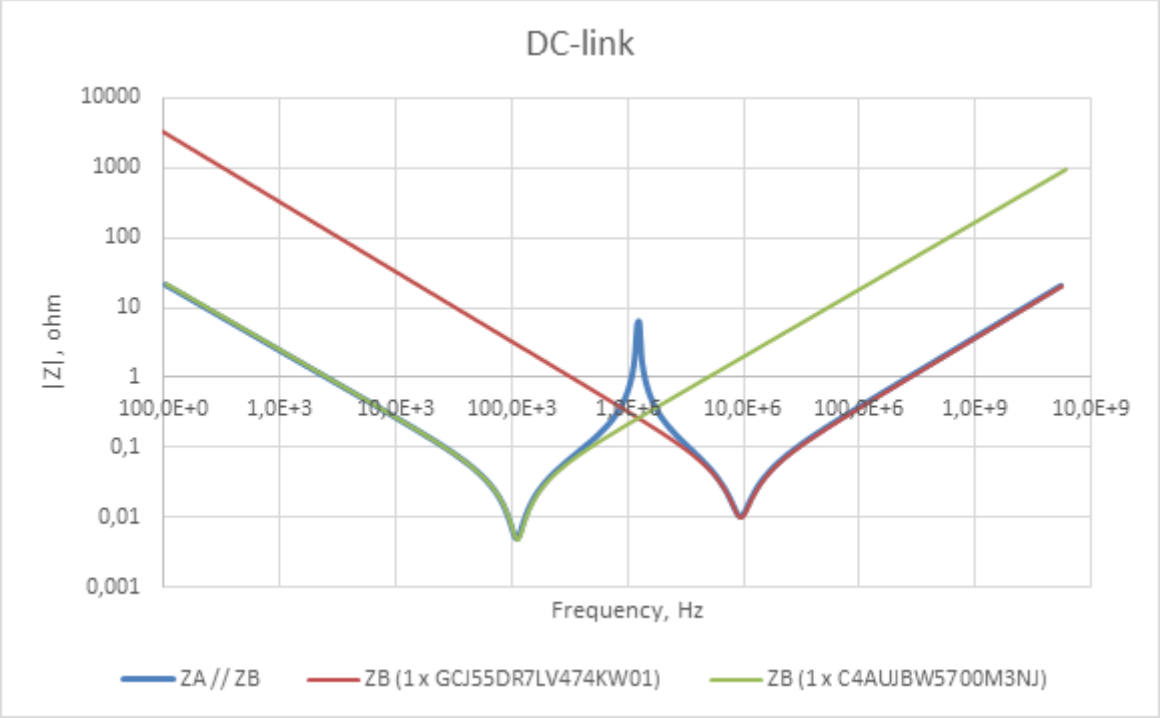

FIGURE 37: FILM AND CERAMIC CAPACITORS IMPEDANCE AND COMBINED DC-LINK IMPEDANCE

The presence of the two capacitors in parallel introduces a resonance around 500kHz that has to be considered to avoid worsening the oscillations generated during the transistor commutation.

8.4.3 EMI Filter

Electromagnetic interference (EMI) generated by power electronic converters is a major concern in modern motor drive and energy conversion systems. Fast switching transitions inherent to PWM inverters produce broadband conducted and radiated disturbances, which may compromise electromagnetic compatibility (EMC) compliance, degrade system reliability, and accelerate component aging. To mitigate these effects, EMI filters are typically employed at both the DC and AC sides of the converter.

DC-side EMI filters are primarily intended to prevent switching noise from propagating back into the supply network. They mainly address common-mode and differential-mode disturbances generated by the inverter, protecting upstream equipment and ensuring compliance with conducted emission standards. These filters usually consist of combinations of capacitors, common-mode chokes, and differential inductances and are often optimized with respect to grid impedance and safety requirements.

AC-side EMI filters, on the other hand, act directly on the inverter output and interface with the motor and connecting cable. In addition to limiting conducted emissions toward the load, AC-side filters play a crucial role in controlling voltage slew rates, reducing insulation stress, mitigating bearing currents, and attenuating radiated emissions caused by long motor cables. Depending on their topology, they may target differential-mode noise, common-mode noise, or both, with varying effectiveness, size, and cost implications.

In the following, the main AC-side filter topologies are reviewed and compared in order to clarify their respective benefits and limitations with respect to EMI mitigation, motor protection, and overall system performance. Several filter topologies can be implemented on the AC side, each with specific advantages and drawbacks. In the following, we focus on the main solutions to highlight their benefits and limitations, namely:

- **In-line chokes**: These components reduce differential-mode noise by increasing the rise time of the voltage pulses, thereby limiting stress on motor insulation. However, they do not mitigate common-mode (CM) electrical noise; as a consequence, cable shielding may still be required to reduce radiated emissions. Moreover, they are ineffective in reducing CM currents flowing through motor bearings.
- **dV/dt filters**: These are low-pass filters inserted in series with each phase, with a cut-off frequency higher than the inverter switching frequency. While effective in limiting voltage slew rate, they do not reduce common-mode electromagnetic interference (CM EMI) and therefore do not prevent CM-current-induced wear of motor bearings.
- **Sine-wave filters**: Based on a topology similar to that of dV/dt filters, sine-wave filters feature a much lower cut-off frequency, typically between the fundamental output AC frequency and the inverter PWM frequency. Nevertheless, common-mode EMI and motor bearing wear are not significantly reduced, meaning that cable shielding is generally still required.
- **Complete filters**: These extend sine-wave filters by adding common-mode chokes and Y-capacitors to also attenuate common-mode currents. While this solution is more effective in reducing CM effects, it comes at the expense of increased size, complexity, and cost.

The noise generated by the system can be then separated into two main components, the so-called *differential mode* (DM), propagated towards the circuit, and the *common mode* (CM), propagated through parasitic couplings. These two noise modes at first can be studied independently. The DM is typically not critical on a power inverter, due to the presence of the DC-link capacitor that filters out

most of the low frequency components (i.e., below few hundreds kHz), but becomes predominant above 1 MHz, where small capacitors connected between DC rails help solving the issue.

Unfortunately, CM noise behaves in the opposite way: it is predominant at low frequency and starts becoming less problematic above few megahertz. In this case CM inductors can be introduced paired with proper capacitors between DC rails and chassis (Y capacitors) to implement a desired filtering circuit.

A simplified equivalent circuit for the CM noise generation and propagation is shown in Figure 38. Studying this circuit enables a proper design of both the DC and AC filters, enabling their optimization from multiple points of view (e.g., component size, cost, effectiveness…).

In this circuit the noise is generated by the switching activity of the power transistors, hence optimizing both their commutation and their coupling to ground will result in reducing the EM noise produced. Focusing on the filter impedances, it is evident that modifying their value can help limiting the noise propagation. The rest of the activity in this task will focus on correctly size and optimize the AC filter.

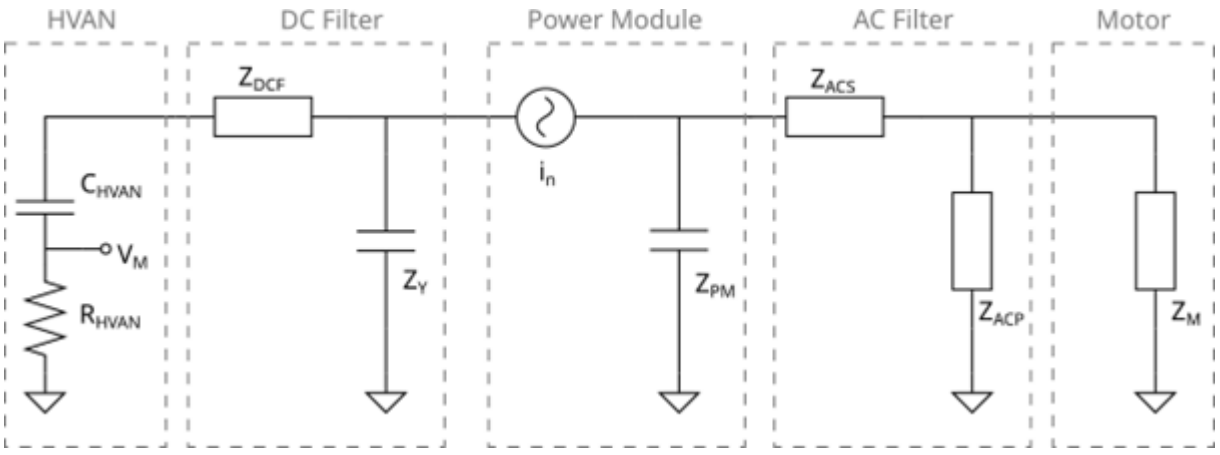

FIGURE 38: EQUIVALENT CIRCUIT FOR CM NOISE

9 High bandwidth current measurement for advanced control strategies in power converters

The activity described in this chapter targets the realization of a current measurement for power converters where high-frequency behaviour of the converter and thus the measurement circuitry is essential. It will be evaluated on a testbench and, if feasible, included in one of the Demos described in the above chapters, probably in Demo 3.1.

With the introduction of GaN semiconductors, the switching frequency range is ever expanding, currently into the multi-megahertz range. This does not stretches the boundaries of the semiconductors itself to the limits, but with that the gate driver circuitry, the control loop, and the required measurements for the input of the control loop. The current measurement is one these measurements that is key in many applications, but the increase in switching frequency of the converter imposes high complexity and instability risks in the current measurement (circuitry).

Another key driver of the increase in switching frequencies is soft-switching of the switches, offering reduced losses and thus potentially higher switching frequencies. In order to fully reach the potential of soft-switching of the switches, especially zero-voltage switching is of the uttermost importance in the multi-MHz range, the direction of the current is very important. Most state-of-the-art power converter use comparators for this type of detection, offering delays in the order of 10 ns, which for a power converter switching at 20 kHz is a fraction, but with the increasing switching frequencies becomes more apparent. Therefore, this demo also targets a advanced phase-delay compensation to reduce the detectable delay in the converter.

9.1 Specification

The specification targets an non-isolated DC-DC converter that is able to transfer 10 kW at 1 kV, such that an average output current of 10 A is required. In order to have sufficient head space for ripple, the maximum peak current is limited at 20 A.

The bandwidth is based on the rule of thumb that the bandwidth of the measurement should be roughly 5 times larger than the signal that it is measuring. Assuming switching times in the order of magnitude of 10 ns, this results in a bandwidth > 175 MHz. Therefore, a minimal bandwidth of 200 MHz is targeted.

In order to reduce the phase-delay in the current measurement, the target is roughly one order of magnitude lower than current comparator circuits.

Parameter		**Value**		**Unit**
	Min.	Nom.	Max.	
Current			20	Apk
Bandwidth	200			MHz
Phase-delay			2	ns

9.2 Research

Although other parameters van be of influence of the operation of a current measurement, the main parameters of interest are the bandwidth, the phase-delay and the desired maximum current. When looking into the research, the main used circuitry for current measurement are:

- Shunt resistance (CVR)
- Hall sensor
- Rogowski coil
- Current transformer

When comparing the state-of-the-art current sensors, the hall sensor and current transformer are not considered due to the limited bandwidth of the sensors itself. This leaves just the shunt resistance and the Rogowski coil as feasible options for the current sensor/measurement circuitry.

9.2.1 Shunt resistance (CVR) measurement

Using a CVR or shunt resistor for high-bandwidth current measurement offers several important advantages when dealing with signals up to and above 200 MHz. First, CVRs provide a highly linear and predictable voltage-to-current relationship, enabling accurate measurements without relying on complex magnetic sensing elements. Their inherently low inductance, especially when using specially designed high-frequency shunt resistor in parallel-series configuration, allows them to preserve fast transient edges and wide-band spectral content while maintaining excellent thermal characteristics. Because they are passive devices, they introduce minimal phase distortion and avoid saturation effects that can occur in magnetic probes. Shunts can also operate over a very wide temperature and current range while maintaining stable characteristics. Additionally, they are compact, inexpensive, and easy to integrate directly into a transmission-line measurement setup, enabling true differential or ground-referenced measurement depending on design. Overall, CVRs offer one of the most reliable ways to capture accurate, high-speed current waveforms with excellent repeatability and bandwidth.

Using a CVR for current measurement at 200 MHz introduces several significant disadvantages. As frequency increases, even extremely small parasitic inductance in the shunt leads or resistor body can cause large measurement errors, distorting both amplitude and phase of the measured waveform. The voltage across the shunt becomes increasingly dominated by $L \cdot \frac{di}{dt}$ rather than $R \cdot I$, limiting accuracy for fast edges. Stray capacitance to ground or adjacent conductors can further alter the effective impedance, creating unwanted resonances and reducing bandwidth. Achieving a truly low-inductance layout requires precise PCB design, controlled geometry, and often specialized RF-grade shunts, increasing complexity and cost. In addition, the very small resistance needed to maintain low inductance results in very low signal levels, which increases sensitivity to noise, amplifier input impedance, and EMI. At these frequencies, maintaining clean Kelvin sensing becomes challenging, and even connector parasitics can compromise fidelity. Overall, while CVRs can work at high bandwidths, 200 MHz operation leaves little margin and demands extremely careful design to avoid significant measurement artefacts.

To summarize: a (combination of) shunt resistors have the potential to achieve very high bandwidth and accuracy over a wide current and/or temperature range. The limitation is mainly the parasitic inductance related to the packaging of the resistor and routing of the PCB.

9.2.2 Rogowski coil measurement

A Rogowski coil offers several advantages for high-frequency current measurement around 200 MHz. Because the coil is air-cored, it has no magnetic saturation, allowing it to handle very large and fast-changing currents without distortion. Its inherently low inductance and wide bandwidth make it well-suited for capturing rapid transients that would overwhelm resistive shunts or magnetic-core sensors. The coil provides excellent galvanic isolation since it does not require insertion into the current path, minimizing disturbance to the circuit under test. Its output is proportional to the derivative of the current, which enhances sensitivity to fast edges and high-frequency components. Additionally, Rogowski coils introduce almost no additional impedance, preserving the original current waveform. Their flexible physical form allows non-intrusive placement around conductors, avoiding PCB layout constraints. Overall, Rogowski coils offer a combination of high bandwidth, isolation, and low disturbance that is difficult to achieve with other current-sensing methods at 200 MHz.

Using a Rogowski coil for current measurement at 200 MHz presents several important drawbacks. At such high frequencies, the coil's self-resonance becomes a limiting factor, causing amplitude distortion and severe phase shift as the operating frequency approaches the resonant point. The coil output naturally decreases with frequency unless carefully compensated, making the signal increasingly small and noise-sensitive. Parasitic capacitance between turns degrades the coil's ideal behavior, introducing unwanted coupling paths and reducing usable bandwidth. The integrator required to reconstruct the current adds additional noise, drift, and bandwidth constraints, making it difficult to preserve the true waveform. Accurate calibration becomes challenging because small variations in coil geometry or placement significantly affect high-frequency performance. Finally, the large loop area makes the coil susceptible to external electromagnetic interference, which becomes increasingly problematic in environments rich in fast switching or RF energy.

To summarize: the Rogowski coil has excellent behavior and has inherent isolation and minimal invasive effects on the converter itself. The limitation mainly lies in the geometry of the windings around the core and potential resonances.

9.2.3 Comparison

A shunt-based current measurement offers better performance at 200 MHz because its behavior remains fundamentally resistive (if properly designed), making its amplitude and phase response much more predictable than that of a Rogowski coil. With a properly designed low-inductance CVR and a high-bandwidth op-amp to amplify the small voltage, the measurement chain can maintain a relatively flat frequency response and "controlled" phase delay that can be corrected analytically or digitally. In contrast, a Rogowski coil begins to suffer severely from parasitic capacitance and self-resonance as frequency approaches the hundreds of megahertz range, causing nonlinear distortion and unpredictable phase shifts. A shunt also provides higher signal levels at high frequency, reducing noise sensitivity and simplifying amplification. Rogowski coils, while non-intrusive and immune to saturation, require an integrator that limits usable bandwidth and introduces its own phase and noise issues. Their output becomes very small at high frequencies, making accurate measurement challenging. Additionally, coil geometry, placement, and mutual

coupling significantly affect performance at 200 MHz, reducing repeatability. In comparison, a shunt offers far more stable calibration and is easier to model mathematically. Overall, for precise waveform fidelity, phase accuracy, and repeatable measurement around 200 MHz, a shunt-based approach is generally superior to a Rogowski coil, despite the latter's advantages in isolation and non-intrusiveness.

A shunt with a wide-bandwidth amplifier delivers far more accurate and predictable current measurements at 200 MHz than a Rogowski coil, which suffers from parasitic-induced amplitude and phase distortion near its self-resonant frequency.

9.3 Simulations

Initial simulation have been set-up to verify different configurations of the CVR in combination with the operational amplifier (and the bandwidth limitations due to the amplifier). Moreover, the effects of parasitic inductances are also being included.

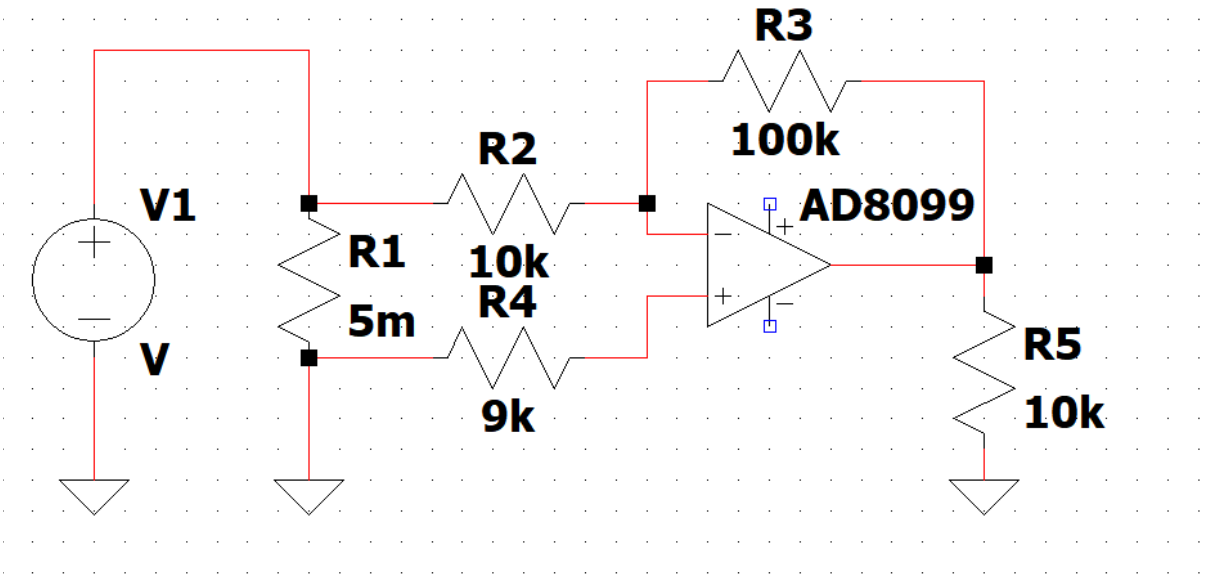

Figure 39: Simplified simulation model.

Due to the expected placement of the resistors, each package adds not only the resistance to the CVR, but also the individual parasitic inductance of the package, but precise placement and the corresponding inductance and resistance will also be taken into account the coming period.

10 Conclusion

10.1 Contribution to overall picture

This document presents an interim progress report about the development of semiconductor devices, sensors and components for safe and efficient e-drives, high-performance batteries with advanced BMS, WBG power inverter systems.

The final conclusions, from the perspective of the contributing partners, are described in the following subsections: the first addresses the state of the art and progress beyond it, the next one outlines the impact on other parts of the project, followed by a subsection detailing contributions to the demonstrations, and finally, an overview of other conclusions and lessons learned.

10.2 Relation to the state of the art and progress beyond it

The following table lists the state of the art related to the work described above and briefly clarifies the plans of progress beyond it by the involved partners.

Partner/Topic	Description
EDI	Increased level of electronics integration and enhanced flexibility of the quantum sensor measurement system.
FAU	Improved quantum sensor sensitivity beyond SotA for comparable endoscopic sensor-heads.
IFAT	Innovative test chip characterisation ongoing, PCB in manufacturing, test benches in development.
I&M	State-of-the-art SiC traction inverters mainly fit two big categories of power stages: six-switches power modules or discrete single switch devices. In the first case the physical dimension and layout of the module limit the space of design solution and geometrical optimization. In the second case, full design flexibility is achieved at the cost of a significant overhead in terms of design effort and complexity. The proposed power stage, based on a half-bridge power module, aims to demonstrate the advantages of this package solution. By jointly optimizing the power modules layout, the DC-link and the cooling system, the design enables reduced switching losses, lower device stress and improve efficiency and power density than current automotive inverter solutions. GaN inverter power stage and DC-link are typically designed to withstand the maximum operating voltage and current. Due to the fast switching provided by the GaN transistors, the stray inductance in the DC-loop has been added as a constraint for this design. Considering both the DC-link and the power stage as a whole, it is possible to optimize the design overall and achieve very fast transitions, reducing the switching losses, limiting both the stress on power transistors and the EM noise generated.
SAL	Introduced an innovative methodology based on FAU quantum sensor to improve both the characterization and the estimation accuracy of Li-ion batteries.
ST-I	ST-I has recently designed state-of-the-art molded MOSFET technology (ACEPACK Gemini, 1200V half-bridge topology) with double-sided cooling for the SiC application and these modules have been selected as building blocks of the inverter to be realized as Demo 3.3, due to their superior thermal performance and reliability.

TU/e	The current research suggest that the shunt resistance measurement with added operational amplifier is still the way to go for a high-bandwidth current sensor. Extensive simulations will be performed and demonstrated to verify the operation and especially the combination with phase-delay compensation to even further reduce the delay between measurement and detection.
TUG	Two test benches were designed which will play a vital part in the development of the metamaterial torque sensor.

10.3 Contribution to demonstrators

The following table briefly describe the relation between this work and the planned demonstrators. Because the overall style of this deliverable is demonstrator/use case oriented, in most cases the partners only state which demonstrators they deal with.

Partner/Topic	Description
EDI	EDI exclusively contributes to Demo 3.2, delivering a quantum sensor based on Nitrogen-Vacancy centres in diamond. However, the advancements in quantum sensing technology will also be demonstrated standalone for exploitation and dissemination purposes.
FAU	FAU contributes the quantum sensor-technology for Demo 3.2 by providing the design and hardware for the fiber-based quantum sensor head. This enables high-precision measurements of magnetic fields, which is critical for the current measurement and future advanced State-of-Health estimation algorithms.
IFAT	IFAT provides the read-out system for the torque sensing principle for Demo 3.1.
I&M	I&M designs a power inverter based on SiC technology (ST-I modules) to be used in Demo 3.3 and another power inverter based on GaN technology as core component of Demo 3.4.
SAL	SAL contributed to Demo 3.2 by using the FAU quantum sensor to characterize Li-ion batteries and provide accurate SoC and SoH estimation. The results demonstrated a strong correlation between the induced magnetic fields and battery state. Ongoing research is focused on further improving the experimental setup and refining the methodology to achieve higher accuracy in estimation parameters.
ST-I	The contribution is related to Demo 3.3 for the development of the power inverter employing the Gemini modules equipped with SiC devices.
TU/e	The contribution consists in delivering a current sensor with high bandwidth and advanced phase-delay compensation.
TUG	Two test benches discs (static and rotational) are developed by TUG to characterize the system consisting of the radar chip and the passive sensor element of the metamaterial in the scope of Demo 3.1.

10.4 Other conclusions and lessons learned

The following table briefly describes other conclusions and learnings derived during the execution of the activities described in this deliverable.

Partner/Topic	Description
I&M	Treating the commutation loop inductance as a primary design constraint proved to be essential to fully exploit the fast switching capability of SiC MOSFETs. This approach directly influenced layout, module selection and DC-link integration. It highlights the strong coupling between electrical performance and mechanical design. The activity confirmed that neglecting parasitic inductance at early design stages leads to limited switching speed or increased device stress, whereas its early control enables improved efficiency, reduced overvoltage and more predictable EMI behavior. The modelling activity performed to guide the design of the power stage and the DC-link has been made using a new simulation software that offers great potential and can ease the simulation activity. Design considerations taken on power loss estimation showed us the advantages and drawbacks of different GaN transistors from the same manufacturer: now it is clear the trade-off between switching losses and conduction losses for the two generations of devices taken into account. Thanks to these findings, the design can be finalized in order to build the prototypes and validate the simulation performed.
SAL	Experimental observations showed that Li-ion batteries contain ferromagnetic materials, which can influence the sensor readings. Selecting appropriate battery materials can help minimize false readings. Additionally, proper shielding is crucial when measuring DC magnetic fields, as surrounding equipment and the motorized stages can significantly affect the sensor measurements.
TU/e	Nothing peculiar so far, but from what is read, the exact placement and extraction of parasitic parameters are key factors for this development.

11 List of abbreviations

AC	Alternating Current
ACIM	AC Induction Motor
AI	Artificial Intelligence
ASIC	Application-Specific Integrated Circuit
ASM	Asynchronous Motors
BMS	Battery Management System
DC	Direct Current
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FEM	Finite Elements Method
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FOC	Field Oriented Control
GaN	Gallium Nitride
KPI	Key Performance Indicator
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
ROS	Robot Operating System
SAW	Surface Acoustic Wave
SiC	Silicon Carbide
SC	Supply Chain
SOH	State of Health
WP	Work Package

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